A Dual-Loop Control to Ensure Fast and Stable Fault-Tolerant Operation of Series Resonant DAB Converters

Pan, Yiwei; Yang, Yongheng; He, Jinwei; Sangwongwanich, Ariya; Zhang, Chenghui; Liu, Yang; Blaabjerg, Frede

Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2020.2975348

Publication date:
2020

Document Version
Accepted author manuscript, peer reviewed version

A Dual-Loop Control to Ensure Fast and Stable Fault-Tolerant Operation of Series Resonant DAB Converters

Yiwei Pan, *Student Member*, *IEEE*, Yongheng Yang, *Senior Member*, *IEEE*, Jinwei He, *Member*, *IEEE*, Ariya Sangwongwanich, *Member*, *IEEE*, Chenghui Zhang, *Senior Member*, *IEEE*, Yang Liu, *Senior Member*, *IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*- When a single-switch open-circuit fault occurs in the series resonant dual-active bridge (SRDAB) converter, the output DC voltage will drop by a half or rise by twice. To maintain continuous power supply, a fault tolerant control method based on the voltage single-loop control is proposed in this paper, where the rectifier-side output square voltage is regulated. Nevertheless, it may excite the resonance between the resonant inductors and DC capacitors, leading to severe low-frequency oscillations, (appearing as the envelope of the high-frequency current). This may trigger the over-current protection and the SRDAB fails to ride through the fault. To address this issue, low-frequency equivalent models are proposed first for the bidirectional power-flow of the SRDAB, enabling frequency-domain analysis of the single-loop voltage control. The analysis reveals that the oscillation depends on the duty-cycle and control parameters, and it is more likely to occur when the converter operates in the boost mode. However, it is not possible to suppress the oscillations by the voltage single-loop control. Thus, a dual-loop fault tolerant control method is developed. The proposed control strategy includes an outer-loop voltage control, an inner-loop current envelope control and a non-linear correction unit. Experimental tests on a 1-kW SRDAB are performed, which validate the effectiveness of the proposal in terms of oscillation suppression.**

***Index Terms*- Series resonant converter, Dual-active-bridge (DAB) converter, Fault tolerant control, Oscillation suppression, DC distribution systems.**

I. INTRODUCTION

High-performance DC/DC converters are needed to enhance the integration and exploitation of DC distribution systems with increasing renewable sources [1]-[9]. Among various DC/DC topologies, the SRDAB converter is promising as an isolated interface in DC distribution systems, as exemplified in Fig. 1. The main advantages of the SRDAB include zero current soft-switching (ZCS) possibility, simple control and bi-directional power flow [7]-[14]. By generating open-loop square waveforms for the H-bridges, the SRDAB operates in the series resonant mode, obtaining a tight coupling between its input and output [7]-[9].

On the other hand, the reliability of power converters is important to guarantee stable operation. Attempts of reliability analysis, fault diagnosis and fault tolerant control have been accordingly made on the SRDAB [16]-[22]. According to [16], 34% of the total converter failures are related to semiconductors. The power device failures can be further categorized into short-circuit faults and open-circuit faults. The short-circuit faults are usually difficult to handle and detect [17], as the fault occurs relatively fast. Thus, the short-circuit fault is typically "protected" through overcurrent devices that shut down the equipment immediately. In contrast, an open-circuit fault may be due to bond wire lift-off or cracks, e.g., thermal cycling effects, gate driver faults, etc [16]-[19]. Although the open-circuit fault does not always immediately trigger protections, the performance of converters will inevitably be deteriorated, possibly leading to permanent failures [17]-[19]. Therefore, fault tolerant control for open-circuit faults should be equipped with the power converters [19]-[21]. Most of the solutions are realized by adding auxiliary switches, redundant circuits, and special control algorithms [19], [20]. The latter one is more cost-effective, as it does not require additional hardware.

In the SRDAB, due to the open-loop control, when a single-switch open-circuit fault happens, the output DC voltage will drop by a half [11]. Although several closed-loop control methods for the SRDAB were developed [13]-[15], in most cases, the SRDAB is open-loop-controlled [2], [7]-[12]. It thus calls for advanced fault-tolerant control strategies to ensure stable operation in the DC distribution systems. Nevertheless, fault tolerant control methods for the SRDAB have been rarely discussed in the literature. For instance, in [10], a fault-tolerant control was proposed for a unidirectional series resonant DC/DC converter, where the rectifier-side is reconfigured to a voltage-doubler rectifier in the case of an open-circuit fault. This strategy was further extended to the

Manuscript received July 14, 2019; revised November 25, 2019, January 9, 2020; accepted February 12, 2020. This paper was supported under the research project – Reliable Power Electronic based Power Systems (REPEPS) by THE VELUX FOUNDATIONS (Award Ref. No.: 00016591). *(Corresponding Author: Yang Liu.)*

Y. Pan, Y. Yang, A. Sangwongwanich, and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg DK-9220, Denmark (e-mail: ypa@et.aau.dk; yoy@et.aau.dk; ars@et.aau.dk; fbl@et.aau.dk).

J. He is with the School of Electrical Automation and Information Engineering, Tianjin University, Tianjin 300072, China (e-mail: jinwei.he@tju.edu.cn.

C. Zhang is with the School of Control Science and Engineering, Shandong University, Jinan 250061, China (e-mail: zchui@sdu.edu.cn).

Y. Liu is with the School of Artificial Intelligence and Automation, Huazhong University of Science and Technology, Wuhan 430074, China (yangliu30@hust.edu.cn)

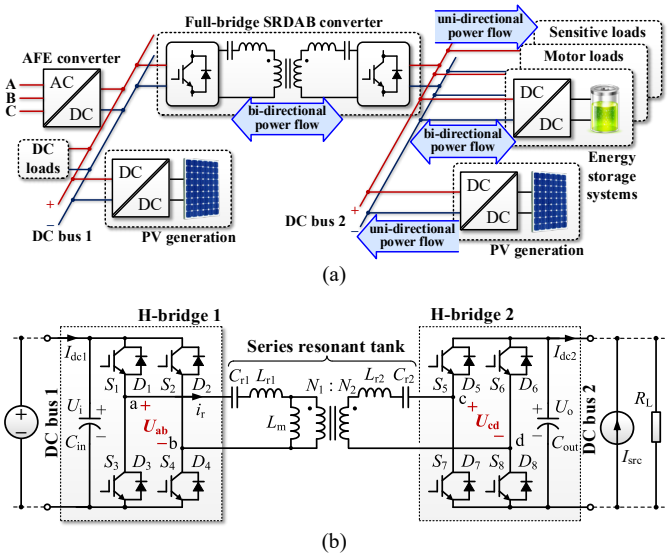


Fig. 1. DC distribution system with series resonant DAB (SRDAB) converters: (a) DC distribution system architecture and (b) circuit diagram of the SRDAB converter.

SRDAB in [11] and [12] to achieve bidirectional fault tolerant capabilities. Although it can effectively improve the fault tolerant capability of the SRDAB, four bidirectional switches and split capacitors at both DC buses are required, increasing the overall cost and complexity. Moreover, in terms of implementation in [12], the overall cost and performance will be compromised. In addition, a surge current may appear during the transient [12]. This may trigger the over-current protection and result in fault tolerant failures [11], [12]. To tackle these, a hybrid fault tolerant method was proposed in [23] without hardware modifications. In this case, the duty-cycle of the rectifier was regulated through a voltage single-loop control. However, the duty-cycle regulation may excite the resonance between the resonant inductors and DC-bus capacitors, and then, un-damped low-frequency oscillations will appear as the envelope of the high-frequency current. This may subsequently trigger the over-current protection.

Moreover, the state-of-art fault tolerant methods for the SRDAB were merely concentrated on one stand-alone converter. Considering the operating conditions of the SRDAB in DC distribution systems, the fault tolerant cases are more complicated. For instance, instead of having a voltage drop by half, the DC voltage may rise by twice after an one-switch open-circuit fault for the SRDAB in DC distribution systems. This may trigger the over-voltage protection eventually. Therefore, it is essential to improve the fault tolerant control in practice.

In light of the above, an improved fault-tolerant method for the SRDAB in DC distribution systems is proposed in this paper, where the oscillation mechanism and its suppression method are addressed. The rest of this paper is organized as follows. Section II introduces the voltage single-loop fault tolerant control method for the SRDAB. In Section III, dynamic equivalent models are proposed for the fault tolerant SRDAB under the duty-cycle regulation for bidirectional power-flow operation. Subsequently, the frequency response

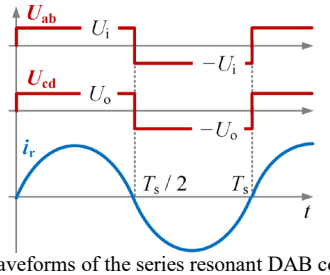


Fig. 2. Operating waveforms of the series resonant DAB converter.

of the system under the voltage single-loop control during fault tolerant operation is analyzed in Section IV. To tackle the issues, a dual-loop control method, consisting of an outer voltage loop, an inner current envelope loop, and a non-linear correction unit, is proposed in Section V. The stability analysis of the proposed method under parameter uncertainties is demonstrated in Section VI. In Section VII, simulation and experimental results are provided to validate the effectiveness of the proposed method before concluding the paper.

II. Voltage Single-Loop Fault Tolerant Method

As exemplified in Fig. 1, an isolated DC/DC converter is adopted to interface DC bus 1 with bus 2. This realizes galvanic isolation and power balance between DC buses, where several distributed loads, sources and energy storage elements are interfaced. The SRDAB is one of the most commonly-used isolated converters in such applications, and according to Fig. 1(b), the resonant frequency f_r can be calculated as

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

where $L_r = L_{r1} + L_{r2}$ and $C_r = C_{r1}C_{r2} / (C_{r1} + C_{r2})$ with L_{r1}, L_{r2} being the resonant inductors and C_{r1}, C_{r2} being the resonant capacitors. The transformer turns-ratio N_1:N_2 is 1:1.

Generally, the SRDAB is controlled with an open-loop system. By generating square waveforms at a switching frequency $f_s = f_r$ for both H-bridges, the converter will operate in the series resonant mode and all power devices commutate at the intervals of zero currents [10], as shown in Fig. 2. In this mode, the SRDAB will tightly couple its input and output voltages with minimum control complexity, and behaves as a "DC transformer" [7]. Ignoring the converter losses, the voltages of both DC buses are identical in steady state. In the distribution system shown in Fig. 1, the voltage of DC bus 1 can be individually controlled by the active-front-end (AFE) converter; or it can be regulated by all DC sources on DC bus 1 through droop control. In contrast, the voltage of DC bus 2 is individually maintained by the SRDAB. In this case, the distributed DC sources on DC bus 2 are current-controlled (e.g., PV converters working in the maximum power point tracking mode), and the DC loads are directly supplied by the SRDAB and the distributed DC energy sources on DC bus 2. The simplified model of this DC distribution system is shown in Fig. 2. If the power generated by the energy sources is lower than the load demand on DC bus 2, the insufficient

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2975348, IEEE Transactions on Power Electronics

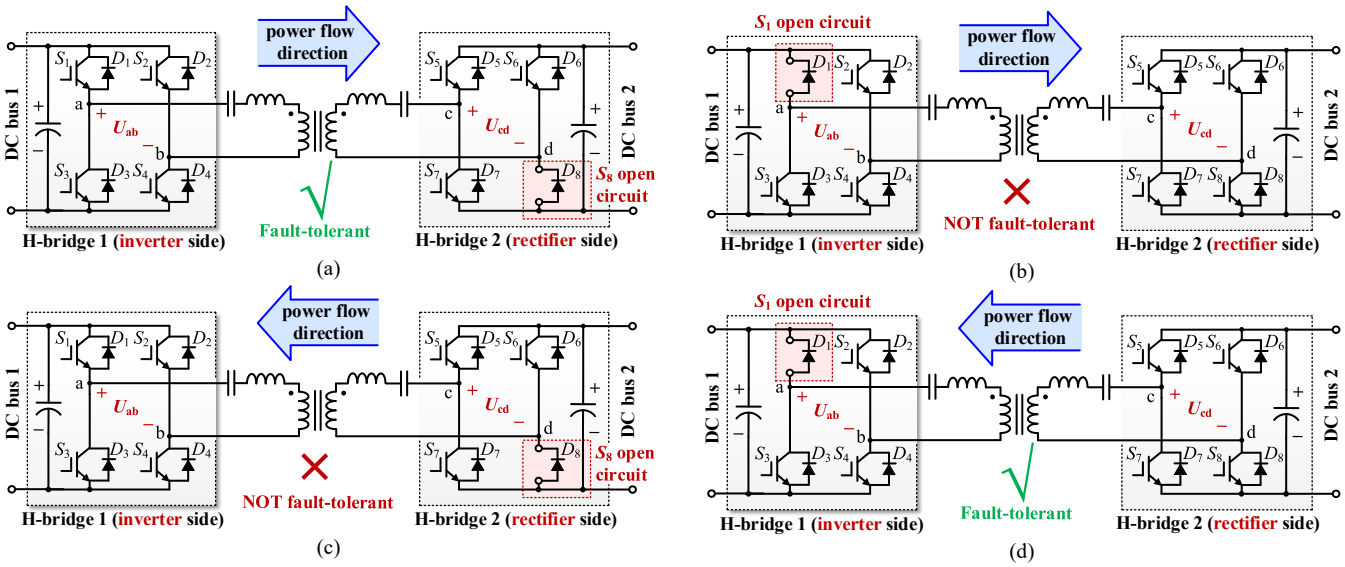


Fig. 3. Open-circuit fault conditions for the SRDAB system: (a) power flows from DC bus 1 to bus 2 with S_8 open-circuited, (b) power flows from DC bus 1 to bus 2 with S_1 open-circuited, (c) power flowing from DC bus 2 to bus 1 with S_8 open-circuited, and (d) power flows from DC bus 2 to bus 1 with S_1 open-circuited.

power is automatically supplied by the SRDAB from DC bus 1 to keep the voltage on DC bus 2 consistent with DC bus 1. If the power generated by the energy sources is higher than the load demand on DC bus 2, the excessive power is delivered to DC bus 1 by the SRDAB. In this way, bidirectional power flow can be achieved. In this paper, the forward power flow direction is defined as the direction for power flowing from DC bus 1 to 2. Then, the SRDAB output voltage corresponds to the voltage of DC bus 2, denoted as U_o.

Although the above control is simple, the fault tolerant capability of the SRDAB is relatively weak. Depending on the power flow direction and the location of the fault switch, the open-circuit faults of the SRDAB can be categorized into four conditions, which are shown in Fig. 3. As observed in Fig. 3(a) and (d), if an open-circuit fault happens in one switch of the rectifier, the rectified DC voltage will not vary significantly, as the freewheeling diodes can still work properly. On the other hand, if an open-circuit fault happens in the inverter, as shown in Fig. 3(b) and (c), the square output of the inverter H-bridge will fall to the half of its normal value. Consequently, for the fault case in Fig. 3(b), the voltage of DC bus 2 will drop by a half [23]. In contrast, it rises to twice of its nominal for the case in Fig. 3(c), because the current source I_{src} will keep charging the capacitors on DC bus 2, until the amplitude of the square voltages of H-bridge 1 and 2 are consistent. Therefore, to address the open-circuit fault issue in the inverter H-bridge, a hybrid fault tolerant method is introduced in the following.

The hybrid fault tolerant method is illustrated with the flow-chart shown in Fig. 4. It first monitors the output DC voltage in real-time according to the current power flow direction. Initially, the SRDAB operates in the open-loop square-wave mode, where the output voltage of the rectifier H-bridge is a 50%-symmetric square waveform and the duty-cycles of H-bridges 1 and 2, denoted as d_1 and d_2, are equal to 1. If a voltage drop or voltage rise on DC bus 2 is detected, the duty-cycle of the output square voltage of the rectifier H-bridge will be regulated by a proportional-integral (PI) controller. More specifically, if the power flows from DC bus 1 to bus 2, and a voltage drop is detected on DC bus 2, d_2 is regulated. Once a voltage rise is detected on DC bus 2, d_1 will be regulated. If an open-circuit fault is confirmed, the regulated duty-cycle d_1 or d_2 should be around 1/3 in steady state [23]. This is to ensure that the fundamental components generated by each H-bridge are identical. If the voltage drop is incurred by other conditions, d_1 or d_2 will be other values in steady state, e.g., still equal to one if the voltage variation is induced by short disturbances of loads. Therefore, depending on the output DC voltage U_o and duty-cycles d_1 and d_2, there are three possible fault tolerant operation conditions:

1) If U_o restores to its nominal range and $(1/3 - d_{th}) < d < (1/3 + d_{th})$ in several consecutive samples, with d_{th} being the threshold of the duty-cycle to categorize the fault conditions, it is assumed that an open-circuit fault occurs in the inverter H-bridge. Then, the rectifier exits the duty-cycle regulation mode at the beginning of the next control period, and is reconfigured as a half-bridge (Stage III in Fig. 4). According to the symmetry of the SRDAB, the rectified DC voltage will still be approximately the same as the input DC voltage in steady state. Moreover, all power devices can still operate in the ZCS mode. This reconfiguration intends to obtain a satisfactory steady-state performance, as the duty-cycle regulation will break the resonant process. The rectifier will switch off at a high current interval, bringing more losses and severe electromagnetic interference [23].

2) If U_o restores to its nominal range and $1 - d_{th} < d \leq 1$ in several consecutive sampling intervals, no open-circuit faults are assumed. The voltage variation may be induced by transient load disturbances. Then, the rectifier exits the duty-cycle regulation mode, and returns to the normal operation mode, where the SRDAB is controlled by an open-loop system and $d_1 = d_2 = 1$.

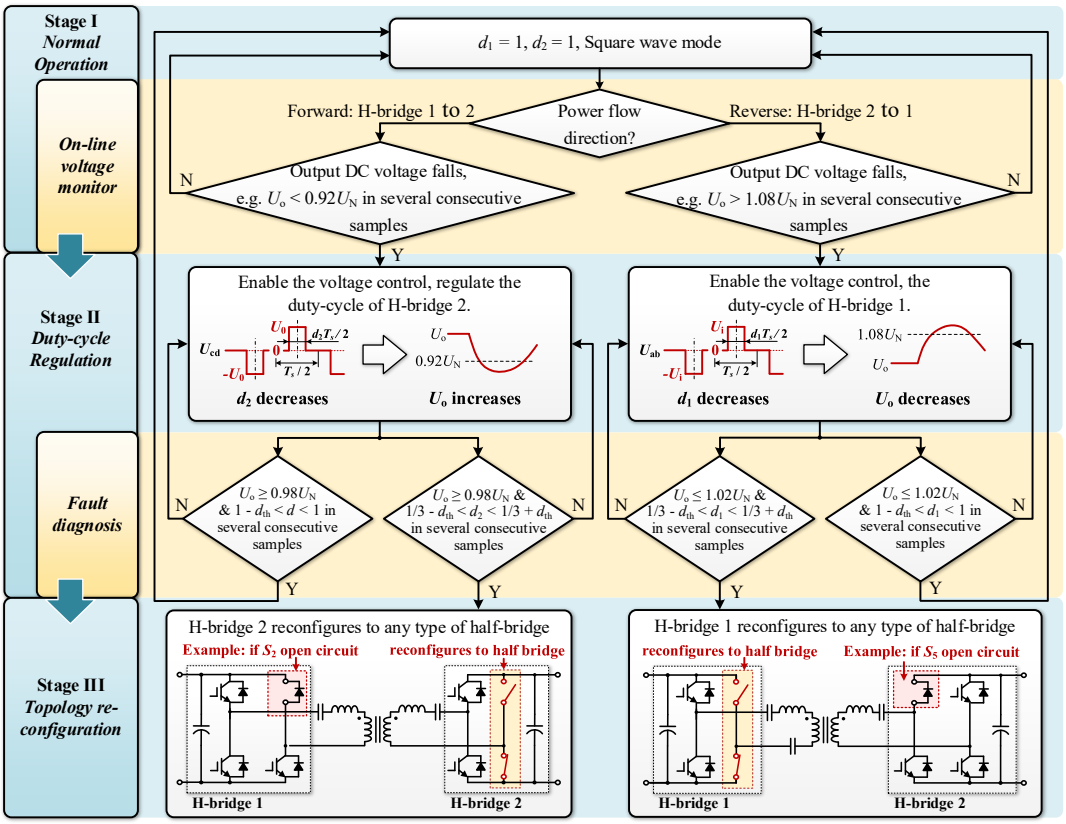


Fig. 4. Flow chart of the fault tolerant control method for the SRDAB.

3) If d has other values in steady state, it is assumed that the voltage variation is the consequence of other failures like inter-turn short-circuit of the transformer and input DC voltage variation, and the converter will keep operating in the duty-cycle regulation mode to sustain the output DC voltage.

Thus, according to the power flow direction, by adjusting the duty-cycles of the rectifier H-bridge in a short period (typically, less than 200 ms) through the voltage closed-loop control, the SRDAB can almost maintain its output voltage. That is, it can achieve the voltage self-restoration and the open-switch-fault self-diagnosis with minimum hardware cost. It should be mentioned that other faults (e.g., the load short-circuit and the converter short-circuit fault) may also affect the rectified DC voltage. In those cases, the over-current protection will be instantly triggered, and thus, they are not considered in the hybrid fault tolerant control method. However, in Fig. 4 (Stage II), the duty-cycle regulation may excite low-frequency oscillations between the resonant inductors and DC-bus capacitors. The oscillations appear as the envelope of the high-frequency current, which may lead to fault tolerant control failures. Its mechanisms will be discussed in the following.

III. Dynamic Equivalent Model under Duty-cycle Regulation

Most of the SRDAB models focus on the power flow, voltage dynamic and soft-switching performances [7], [8], [14], [15], where the duty-cycle is usually fixed. To develop a model that is able to mimic the behavior of the actual system, the steady-state operational waveforms of the SRDAB should be analyzed.

The steady-state voltage and current of the SRDAB under the duty-cycle regulation are illustrated in Fig. 5, where the bidirectional power-flow cases are considered. As observed in Fig. 5, the output voltage of the inverter, i.e., U_{ab} in Fig. 5(a) and U_{cd} in Fig. 5(b), is halved. The duty-cycle of the rectifier is regulated. Accordingly, for the forward power flow, the fundamental components of U_{ab} and U_{cd}, denoted as $U_{ab,f}$ and $U_{cd,f}$, can be described as

$$U_{ab,f} = \frac{4}{\pi}\left(\frac{1}{2}U_i\right)\sin\omega_s t,\ U_{cd,f} = \frac{4}{\pi}U_o \sin\frac{d_2\pi}{2}\sin\omega_s t \qquad (2)$$

For the reverse power flow, $U_{ab,f}$ and $U_{cd,f}$ can be described as

$$U_{ab,f} = \frac{4}{\pi}U_i \sin\frac{d_1\pi}{2}\sin\omega_s t,\ U_{cd,f} = \frac{4}{\pi}\left(\frac{1}{2}U_o\right)\sin\omega_s t \qquad (2)$$

where $\omega_s = 1/\sqrt{L_r C_r}$ is the switching frequency. To sustain the output DC voltage, $U_{ab,f}$ and $U_{cd,f}$ should be identical. Therefore, d_1 or d_2 equals to 1/3 in steady state. With the duty-cycle regulation, the entire resonance cannot be maintained, and thus, the high-frequency current i_r becomes non-sinusoidal. The fundamental component of i_r, denoted as $i_{r,f}$, is also depicted in Fig. 5. It should be noted that under various switch fault conditions, only the DC-bias of the inverted

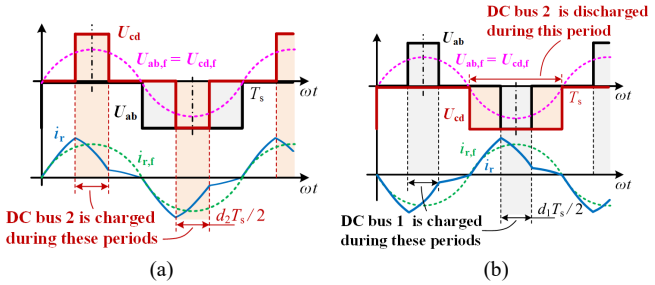


Fig. 5. Steady-state voltage and current of the SRDAB under the duty-cycle regulation: (a) when S_1 is open-circuited and power flows from H-bridge 1 to H-bridge 2, and (b) when S_5 is open-circuited and power flows from H-bridge 2 to H-bridge 1.

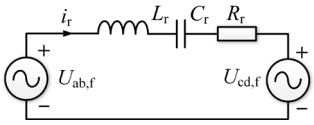


Fig. 6. Conventional equivalent circuit model for the SRDAB.

square voltage are changed, while the shapes of other voltages and the currents are identical for a constant d, as the resonant capacitors have blocked the DC component of the inverted voltage. Thus, in this paper, only the two cases shown in Fig. 5 are analyzed.

A fundamental equivalent circuit can be then developed to study the characteristics of the SRDAB, as shown in Fig. 6. However, it is not sufficient to reveal the low-frequency oscillations, since the conventional model is only validate to analyze the characteristics near the switching frequency. Based on the converter features, a DC model is developed, as shown in Fig. 7 for the forward power flow and Fig. 8 for the reverse power flow. For simplicity, in the models, only the fundamental components ($U_{ab,f}$, $U_{cd,f}$ and $i_{r,f}$ in Fig. 5) are considered [24], which are illustrated in detail.

A. Forward Power Flow

In the case of the forward power flow, the AC sources (see Fig. 6) are replaced by two DC voltage sources, whose amplitudes are $\frac{\sqrt{2}U_i}{\pi}$ and $\frac{2\sqrt{2}U_o}{\pi}\sin\frac{d_2\pi}{2}$, respectively. An inductor L_{dc} is added between the two DC sources, as shown in Fig. 7(a). The stored energy in L_{dc} and the resonant tank should be the same, i.e., $L_{dc} = \frac{\pi^2}{4}L_r$, according to [7]. A series resistor R_{loss} is also included, which is used to emulate the converter losses of the power semiconductors. The average inductor current of this model, denoted as $i_{r,avg}$, can be used to study the low-frequency behavior of the high-frequency current i_r in the SRDAB. It can be further observed in Fig. 7 that a controlled current source circuit is considered to explore the DC terminal behavior. In Fig. 7(b), $C_{dc} = C_{out}$, and R_L is the load of DC bus 2. As shown in Fig. 5(a), the SRDAB converter charges the rectifier DC capacitor for an interval of d_2T_s in every switching cycle, with T_s being the switching period. Thus, the controlled DC current is proportional to the average current $i_{r,avg}$, represented by $mi_{r,avg}$, and the proportional coefficient m can be approximated as

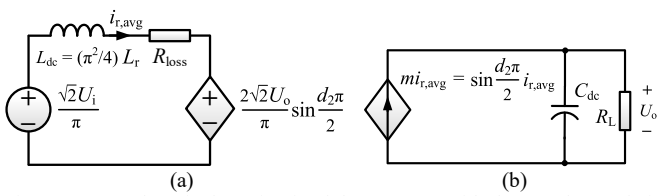


Fig. 7. Proposed equivalent circuit of the SRDAB with duty-cycle regulation for the forward power flow: (a) controlled voltage source circuit and (b) controlled current source circuit.

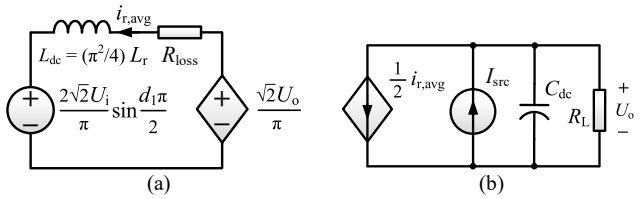


Fig. 8. Proposed equivalent circuit of the SRDAB with duty-cycle regulation for the reverse power flow: (a) controlled voltage source circuit and (b) controlled current source circuit.

$$m = \frac{\frac{2}{d_2T_s}\int_{\frac{T_s}{4}-\frac{d_2T_s}{4}}^{\frac{T_s}{4}+\frac{d_2T_s}{4}} i_{r,f}\,dt}{\frac{2}{d_2T_s}\int_0^{\frac{T_s}{2}} i_{r,f}\,dt} = \sin\frac{d_2\pi}{2} \tag{3}$$

Accordingly, the equivalent circuit for the forward power flow is obtained, as shown in Fig. 7, where the amplitude of the input DC source drops by a half due to the fault. Subsequently, the state-space model can be expressed as

$$\begin{bmatrix}\dot{i}_{r,avg}\\ \dot{u}_o\end{bmatrix} = \begin{bmatrix}-\frac{4R_{loss}}{\pi^2L_r} & -\frac{8\sqrt{2}\sin\frac{d_2\pi}{2}}{\pi^3L_r}\\ \frac{\sin\frac{d_2\pi}{2}}{C_{dc}} & -\frac{1}{R_LC_{dc}}\end{bmatrix}\begin{bmatrix}i_{r,avg}\\ u_o\end{bmatrix} + \begin{bmatrix}\frac{8\sqrt{2}}{\pi^3L_r}\\ 0\end{bmatrix}\left(\frac{1}{2}u_i\right) \tag{4}$$

where the state variables are $x^T = [i_{r,avg},\ u_o]^T$. Let $i_{r,avg} = I_{r,avg} + \hat{i}_{r,avg}$, $u_o = U_o + \hat{u}_o$, $u_i = U_i + \hat{u}_i$, $d_2 = D_2 + \hat{d}_2$, and $\sin(\pi/2)\hat{d}_2 \approx (\pi/2)\hat{d}_2$, which are substituted into (5), and then, after several derivations, the small-signal state-space model can be obtained as

$$\begin{aligned}\begin{bmatrix}\dot{\hat{i}}_{r,avg}\\ \dot{\hat{u}}_o\end{bmatrix} &= A\hat{x} + B\hat{u}_i + K\hat{d} = \begin{bmatrix}-\frac{4R_{loss}}{\pi^2L_r} & -\frac{8\sqrt{2}\sin\frac{D_2\pi}{2}}{\pi^3L_r}\\ \frac{\sin\frac{D_2\pi}{2}}{C_{dc}} & -\frac{1}{R_LC_{dc}}\end{bmatrix}\begin{bmatrix}\hat{i}_{r,avg}\\ \hat{u}_o\end{bmatrix} + \begin{bmatrix}\frac{4\sqrt{2}}{\pi^3L_r}\\ 0\end{bmatrix}\hat{u}_i\\ &+ \frac{\cos\frac{D_2\pi}{2}}{2\sqrt{2}R_L\sin^2\frac{\pi}{2}D_2 + \pi R_{loss}}\begin{bmatrix}-\frac{8R_LU_i\sin\frac{\pi}{2}D_2}{\pi^2L_r}\\ \frac{\sqrt{2}\pi U_i}{2C_{dc}}\end{bmatrix}\hat{d}_2\end{aligned} \tag{5}$$

where D_2 refers to the steady-state value of the duty-cycle d. The steady-state values $[I_{r,avg},\ U_o]^T$ can be expressed as

$$\begin{bmatrix}I_{r,avg} & U_o\end{bmatrix}^T = -A^{-1}BU_i = \frac{\begin{bmatrix}\sqrt{2}U_i & \sqrt{2}R_LU_i\sin\frac{\pi}{2}D_2\end{bmatrix}^T}{2\sqrt{2}R_L\sin^2\frac{\pi}{2}D_2 + \pi R_{loss}} \tag{6}$$

If R_{loss} is ignored, $U_{\text{o}} = U_{\text{i}} / (2\sin\frac{\pi}{2}D_2)$. Therefore, when $D_2 = 1/3$, $U_{\text{o}} = U_{\text{i}}$, and the converter works in the boost mode. This result is in accordance with the experimental results provided in [23].

B. Reverse Power Flow

For the reverse power flow, the AC sources in Fig. 6 are also replaced by two DC voltage sources, whose amplitudes are $\frac{2\sqrt{2}U_{\text{i}}}{\pi}\sin\frac{d_1\pi}{2}$ and $\frac{\sqrt{2}U_{\text{o}}}{\pi}$, respectively. The same DC inductor L_{dc} and series resistor R_{loss} are added, as shown in Fig. 8. The controlled current source will become (½)$i_{\text{r,avg}}$, as the DC bus 2 is discharged in every half switching period, as shown in Fig. 5(b). Moreover, a DC current source I_{src} is added to mimic the behavior of the current-controlled distributed energy source on DC bus 2. Subsequently, the state-space model for the reverse power flow can be expressed as

$$\begin{bmatrix}\dot{i}_{\text{r,avg}}\\ \dot{u}_{\text{o}}\end{bmatrix}=\begin{bmatrix}-\frac{4R_{\text{loss}}}{\pi^2L_r} & \frac{4\sqrt{2}}{\pi^3L_{\text{r}}}\\ -\frac{1}{2C_{\text{dc}}} & -\frac{1}{R_{\text{L}}C_{\text{dc}}}\end{bmatrix}\begin{bmatrix}i_{\text{r,avg}}\\ u_{\text{o}}\end{bmatrix}+\begin{bmatrix}-\frac{8\sqrt{2}}{\pi^3L_{\text{r}}}\sin\frac{d_1\pi}{2} & 0\\ 0 & \frac{1}{C_{\text{dc}}}\end{bmatrix}\begin{bmatrix}u_{\text{i}}\\ i_{\text{src}}\end{bmatrix} \tag{7}$$

Then, the small-signal state-space model can be obtained as

$$\begin{bmatrix}\dot{\hat{i}}_{\text{r,avg}}\\ \dot{\hat{u}}_{\text{o}}\end{bmatrix}=\begin{bmatrix}-\frac{4R_{\text{loss}}}{\pi^2L_r} & \frac{4\sqrt{2}}{\pi^3L_{\text{r}}}\\ -\frac{1}{2C_{\text{dc}}} & -\frac{1}{R_{\text{L}}C_{\text{dc}}}\end{bmatrix}\begin{bmatrix}\hat{i}_{\text{r,avg}}\\ \hat{u}_{\text{o}}\end{bmatrix}+\begin{bmatrix}-\frac{8\sqrt{2}\sin\frac{\pi}{2}D_1}{\pi^3L_r} & 0\\ 0 & \frac{1}{C_{\text{dc}}}\end{bmatrix}\begin{bmatrix}\hat{u}_{\text{i}}\\ \hat{i}_{\text{src}}\end{bmatrix}+\begin{bmatrix}-\frac{4\sqrt{2}U_i\cos\frac{\pi}{2}D_1}{\pi^2L_{\text{r}}}\\ 0\end{bmatrix}\hat{d}_1 \tag{8}$$

The steady-state values $[I_{\text{r,avg}},\ U_{\text{o}}]^T$ can be expressed as

$$\begin{bmatrix}I_{\text{r,avg}} & U_{\text{o}}\end{bmatrix}^T=-A^{-1}BU_{\text{i}}=\frac{\begin{bmatrix}-2\sqrt{2}\sin\frac{\pi}{2}D_1U_{\text{i}}+\sqrt{2}I_{\text{src}}R_{\text{L}}\\ \sqrt{2}\sin\frac{\pi}{2}D_1U_{\text{i}}R_{\text{L}}+\pi I_{\text{src}}R_{\text{L}}R_{\text{loss}}\end{bmatrix}}{\pi R_{\text{loss}}+\frac{\sqrt{2}}{2}R_{\text{L}}} \tag{9}$$

If R_{loss} is ignored, $U_{\text{o}} = 2\sin(\pi/2)D_1U_{\text{i}}$. Thus, when $D_2 = 1/3$, $U_{\text{o}} = U_{\text{i}}$, and the converter will operate in the buck mode.

According to (5) and (8), the transfer function of $i_{\text{r,avg}}(s)$ and $u_{\text{o}}(s)$ in respect to the duty-cycle $d_1(s)$ and $d_2(s)$, denoted as $G_{\text{ird1}}(s)$, $G_{\text{ird2}}(s)$, $G_{\text{ud1}}(s)$ and $G_{\text{ud2}}(s)$, can be obtained. To validate the accuracy of the proposed models, the frequency domain responses between the proposed model and a circuit simulation model in MATLAB/Simulink are compared in Fig. 9. The Bode plots of $G_{\text{ird1}}(s)$, $G_{\text{ird2}}(s)$, $G_{\text{ud1}}(s)$ and $G_{\text{ud2}}(s)$ are shown in solid lines. The frequency-response results in simulations are obtained through perturbing the duty-cycle D_1 and D_2 with a frequency sweeping signal whose amplitude is 0.03 and ranging from 10 ~ 5×10^3 rad/s. Then, the fast Fourier transform (FFT) is applied to the output signals (u_{o} and the absolute average value of i_{r}) to obtain the frequency-domain responses, which are shown in " * " in Fig. 9. The simulation parameters are listed in Table I.

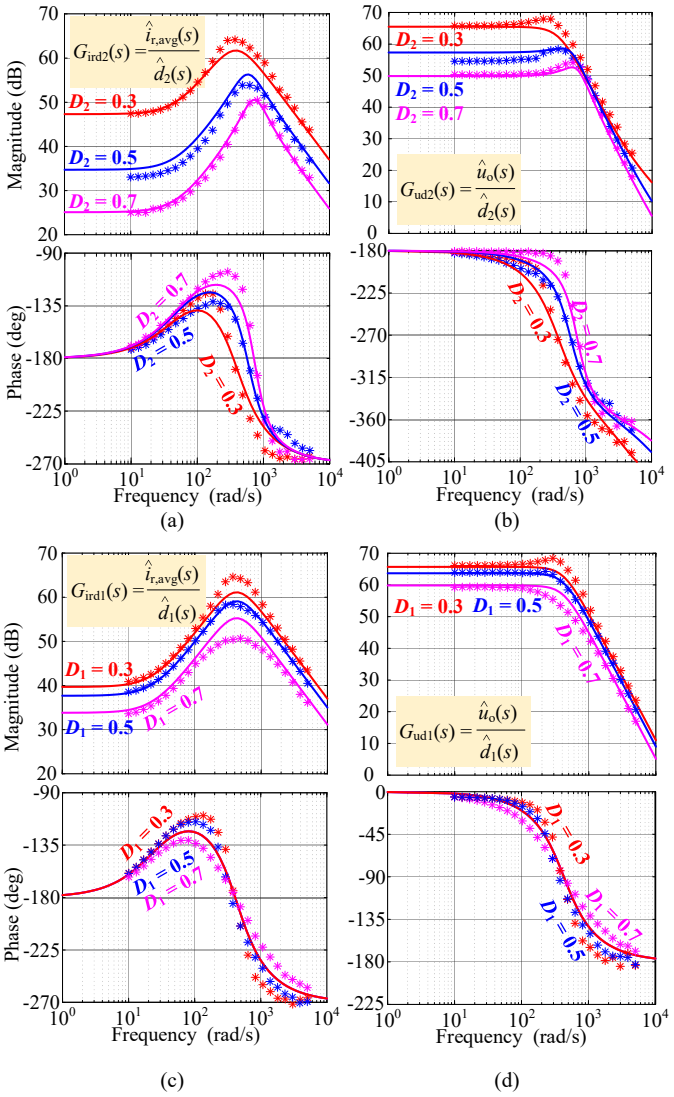


Fig. 9. Frequency responses of the simulation model (*) and the proposed model (solid lines) under various steady-state duty-cycles D_1 and D_2: (a) Bode plots of $G_{\text{ird2}}(s)$, (b) Bode plots of $G_{\text{ud2}}(s)$, (c) Bode plots of $G_{\text{ird1}}(s)$, and (b) Bode plots of $G_{\text{ud1}}(s)$. Here, $\hat{d}_1(s)$ and $\hat{d}_2(s)$ are the disturbances of the duty-cycle D_1 and D_2, $\hat{i}_{\text{r,avg}}(s)$ is the disturbance of the current through L_{dc}, and $\hat{u}_0(s)$ is the disturbance of the output voltage. The amplitude of $\hat{d}_1(s)$ and $\hat{d}_2(s)$ are both 0.03.

As it can be observed in Fig. 9, the proposed model (Figs. 7 and 8) and the simulation model exhibit similar characteristics in the frequency range of 10 to 5×10^3 rad/s, which means that the proposed equivalent model shown in Figs. 7 and 8 can be used to study the behavior of the SRDAB under the fault-tolerant operation in the low frequency domain.

For the forward power flow, it should be noted that the magnitude responses $G_{\text{ird2}}(s)$ under various static duty-cycles D_2 have peaks around 300 to 800 rad/s. More importantly, these peaks vary with the steady-state duty-cycles, which is very similar to the conventional DC/DC boost converter [25]. Additionally, the damping ratios change slightly with D. On the other hand, as shown in Fig. 9(b), the magnitude responses of $G_{\text{ud2}}(s)$ are relatively flat, which means that the oscillation

TABLE I. SIMULATION PARAMETERS OF THE SRDAB.

Circuit parameters	Value
Nominal DC voltages U_i, U_o	750 V
DC capacitance C_{in}, $C_{out} = C_{dc}$	1000 μF
Transformer ratio N_1:N_2	1:1
Load of DC bus 2 R_L	40 Ω
Resonant capacitors C_{r1}, C_{r2}	4 μF
Resonant inductors L_{r1}, L_{r2}	27 μH
Switching frequency f_s	4.8 kHz
Magnetic inductance of HF transformer L_m	19.9 mH
Series resistor R_{loss}	0.8 Ω
Current source in DC bus 2 I_{src} (for the reverse power flow)	40 A

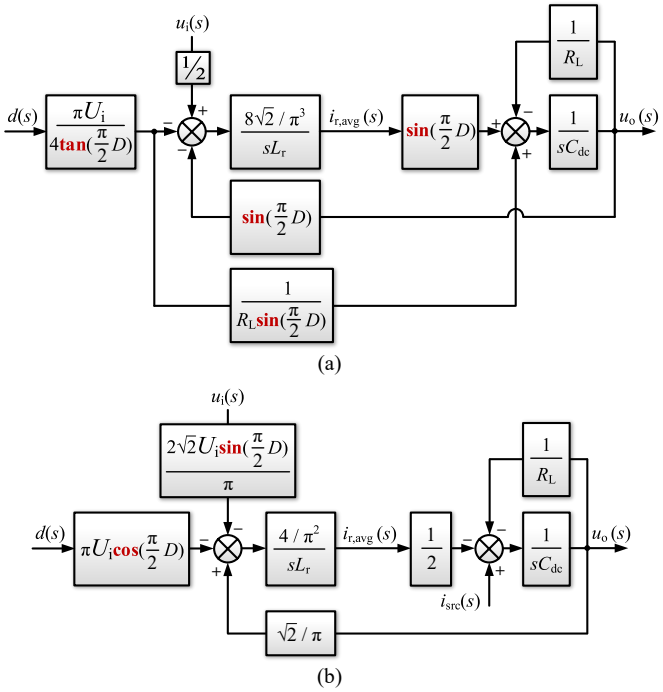


Fig. 10. Block diagrams of the proposed equivalent model for the SRDAB converter in (a) the forward power flow mode and (b) the reverse power flow mode.

induced by the resonant inductors and DC capacitors is not likely to emerge in the output DC voltage.

Comparing to the forward power flow where the frequency response of $G_{ird2}(s)$ varies greatly with different duty-cycles, the frequency response of $G_{ird1}(s)$ moves slightly higher in amplitude with the decrease of duty-cycle D_1 as shown in Fig. 9(c) and (d). The peaks of $G_{ird1}(s)$ under various static duty-cycles D_1 have the same frequency. Similar to the forward power flow, the magnitude responses of $G_{ud1}(s)$ are also very flat (see Fig. 9(d)).

Nevertheless, differences also present between the proposed model and the simulated model. For example, for the forward power flow, when D_2 = 0.3, the simulation model shows a higher resonant peak, as it can be observed in Fig. 9(a) and (b). For the reverse power flow, the simulation model presents a duty-cycle-dependent damping ratio, which grows larger with the increase of the duty-cycle D_1. The inaccuracies may be due to: 1) the fundamental component of the high-frequency current $i_{r,f}$ is employed to approximate the non-sinusoidal current i_r; 2) with the variation of the duty-cycle, the rectifier power devices are switched off under different currents, leading to variable switching losses and a variable resistance R_{loss} in the model; 3) the dead-time effect was not considered in the proposed model; 4) the magnetizing current of the high-frequency transformer was neglected. Although those characteristics are difficult to be reflected in the model, it is sufficient to approximate the features of the SRDAB with the duty-cycle regulation in the low frequency region. That is, the model is effective to analyze the dynamics of the SRDAB.

For simplicity, assuming that R_{loss} = 0, for the forward power flow, the transfer functions $G_{ird2}(s)$ and $G_{ud2}(s)$ can be obtained through $G_{xd}(s) = (sI - A)^{-1}K$ as

$$\begin{bmatrix} G_{ird2}(s) \\ G_{ud2}(s) \end{bmatrix} = \frac{\begin{bmatrix} -\frac{2\sqrt{2}U_i}{\pi^2 L_r \tan\frac{D_2\pi}{2}}\left(s+\frac{2}{R_L C_{dc}}\right) \\ \frac{U_i\cos\frac{D_2\pi}{2}}{C_{dc}}\left[\frac{\pi}{4R_L\sin^2\frac{D_2\pi}{2}}s-\frac{2\sqrt{2}}{\pi^2 L_r}\right] \end{bmatrix}}{s^2+\left(\frac{1}{R_L C_{dc}}\right)s+\frac{8\sqrt{2}\sin^2\frac{D_2\pi}{2}}{\pi^3 L_r C_{dc}}} \tag{10}$$

For the reverse power flow case, the transfer functions $G_{ird1}(s)$ and $G_{ud1}(s)$ can be obtained as

$$\begin{bmatrix} G_{ird1}(s) \\ G_{ud1}(s) \end{bmatrix} = \frac{-\frac{4\sqrt{2}U_i\cos\frac{D_1\pi}{2}}{\pi^2 L_r}\begin{bmatrix} s+\frac{1}{R_L C_{dc}} & -\frac{1}{2C_{dc}} \end{bmatrix}^T}{s^2+\left(\frac{1}{R_L C_{dc}}\right)s+\frac{2\sqrt{2}}{\pi^3 L_r C_{dc}}} \tag{11}$$

Referring to the Bode plots in Fig. 9, Eqs. (10) and (11) reveals that the system is a second-order system. Compared with the typical second-order system, it is known that:

1) There is a resonant point between the resonant inductor and DC capacitor, which moves to the high-frequency region with the increase of D_2 for the forward power flow, while it remains constant in the reversed power flow mode.
2) Since $G_{ud2}(s)$ has a right-half plane (RHP) zero, for the forward power flow case, the system is a non-minimum-phase system.
3) For the forward power flow, the system damping ratio decreases with the increase of the duty-cycle D_2.

With the above analysis, the proposed model can be represented as shown in Fig. 10, according to the state-space model in Eqs. (5) and (8). For the forward power flow, the SRDAB operates in the boost mode, and its transfer functions are similar to those for the conventional DC/DC boost converter. For the reverse power flow, the SRDAB operates in the buck mode, and its characteristics are similar to the conventional DC/DC buck converter. However, the SRDAB system is highly nonlinear, as indicated by Fig. 10. Therefore, in the forward power flow mode, the fault tolerant operation of the SRDAB is a nonlinear, parameter-variant, non-minimum-phase second-order system. This characteristic will bring difficulties to design the controller. On the other hand, in the

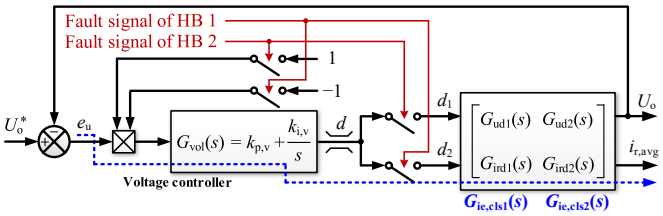


Fig. 11. Control diagram of the voltage single-loop fault tolerant method.

case of the reverse power flow, the system is a nonlinear, parameter-invariant, minimum-phase second-order system, where the controller design is easier. In all, to ensure the stable operation of the SRDAB under open-circuit faults, the characteristics under the voltage single-loop control should be studied.

IV. Characteristics under the Voltage Single-Loop Fault Tolerant Method

In the voltage single-loop fault tolerant method, a voltage PI regulator is implemented to control the rectified DC voltage, when the open-circuit fault happens. The control diagram is shown in Fig. 11, where $G_{vol}(s)$ is the transfer function of the PI voltage regulator with $k_{p,v}$ and $k_{i,v}$ being its proportional and integral gains. Since the increase of d_2 will decrease the output DC voltage for the forward power flow case, a negative unity gain should be multiplied with the output of the PI regulator. However, whether this voltage single-loop control is capable to suppress the low-frequency oscillations or not is further detailed in this section.

A. Forward Power Flow (Boost Mode)

The frequency response of the open-loop system $G_{vol}(s)\cdot G_{ud2}(s)$ in this case is shown in Fig. 12. As it can be seen in Fig. 12(a), the increase of D_2 will lower the magnitude of $G_{vol}(s)\cdot G_{ud2}(s)$. In contrast, the increase of $k_{p,v}$ and $k_{i,v}$ leads to higher magnitudes of the open-loop system in the high and low frequency bands, respectively, as shown in Fig. 12(b) and (c). When $k_{p,v}$ = 0.005, $k_{i,v}$ = 0.13, the cut-off frequency is around 1000 rad/s, and the phase margin γ is larger than 14° with D = 0.3 ~ 0.7, indicating that the system is stable. With larger $k_{p,v}$, the system can acquire higher voltage control bandwidth, which means lower voltage drop can be obtained at the beginning of the fault tolerant control. With larger $k_{i,v}$, the fault tolerant duration time can be shortened, since the system will enter into the steady-state faster. However, owing to the non-minimum-phase features, larger $k_{p,v}$ and $k_{i,v}$ will significantly decrease the phase margin of the system, leading to poorer stability performances. On the contrary, smaller $k_{p,v}$ and $k_{p,i}$ will slow down the dynamics. Therefore, the PI parameters should be tuned in consideration of the fault tolerant control performances and stability.

To explore the characteristics of the average inductor current $i_{r,avg}(s)$ with the voltage single-closed-loop control, the frequency responses of $G_{ie,cls}(s)$ = $i_{r,avg}(s)$ / $e_u(s)$ (shown in dashed lines in Fig. 11), with $e_u(s)$ being the DC voltage error, are given in Fig. 13 with the same control parameters. It can

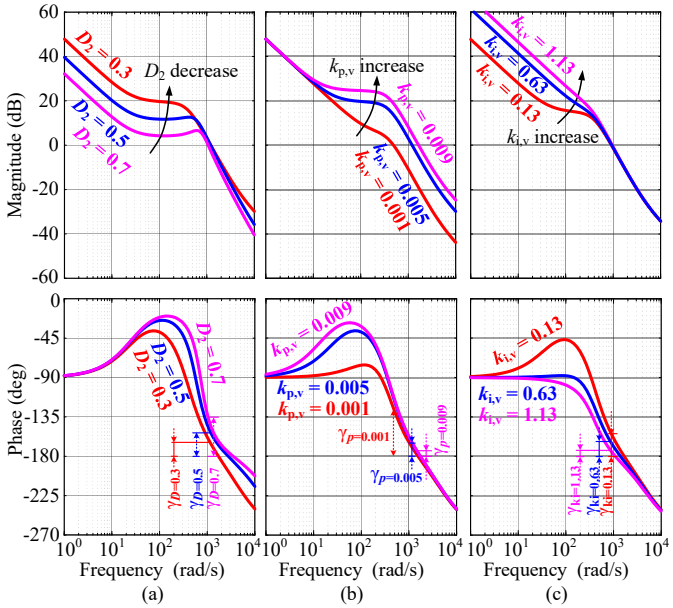


Fig. 12. Frequency responses of the open-loop system in fault tolerant operation for the forward power flow: (a) when $k_{p,v}$ = 0.005, $k_{i,v}$ = 0.13, (b) when D_2 = 0.3, $k_{i,v}$ = 0.13, and (c) when D_2 = 0.3, $k_{p,v}$ = 0.003.

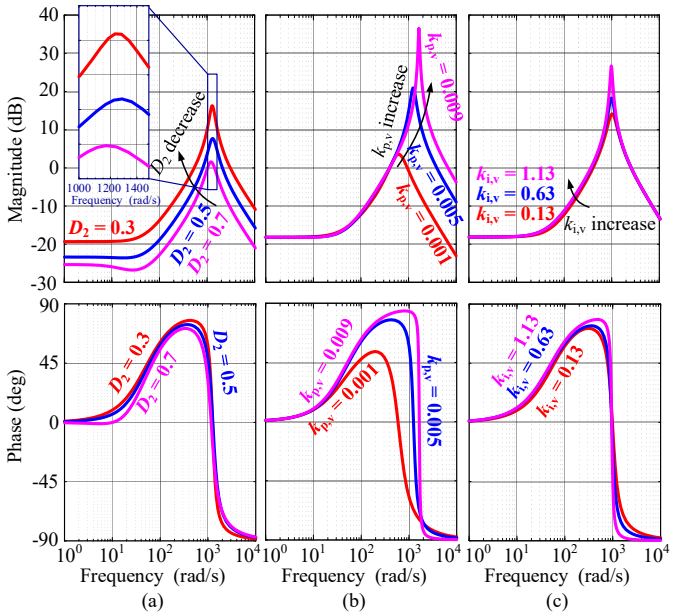


Fig. 13. Frequency responses of the closed-loop system in fault tolerant operation for the forward power flow: (a) when $k_{p,v}$ = 0.005, $k_{i,v}$ = 0.13, (b) when D_2 = 0.3, $k_{i,v}$ = 0.13, and (c) when D_2 = 0.3, $k_{p,v}$ = 0.003.

be seen in Fig. 13(a) that $G_{ie,cls}(s)$ has a peak with the frequency around 1200 rad/s. Moreover, the resonant peak becomes higher in amplitude with the decrease of D_2, and the frequency also varies. When $k_{p,v}$ increases, the resonant frequency will increase, as demonstrated in Fig. 13(b). In addition, the increase of $k_{p,v}$ or $k_{i,v}$ will increase and sharpen the peaks of the frequency responses, as shown in Fig. 13(b) and (c). Therefore, it is implied in Fig. 12 that even when the system is stable under the voltage single-closed-loop control, the PI voltage controller is not able to suppress the resonance. In this case, during the transition to fault tolerant operation, a

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2975348, IEEE Transactions on Power Electronics

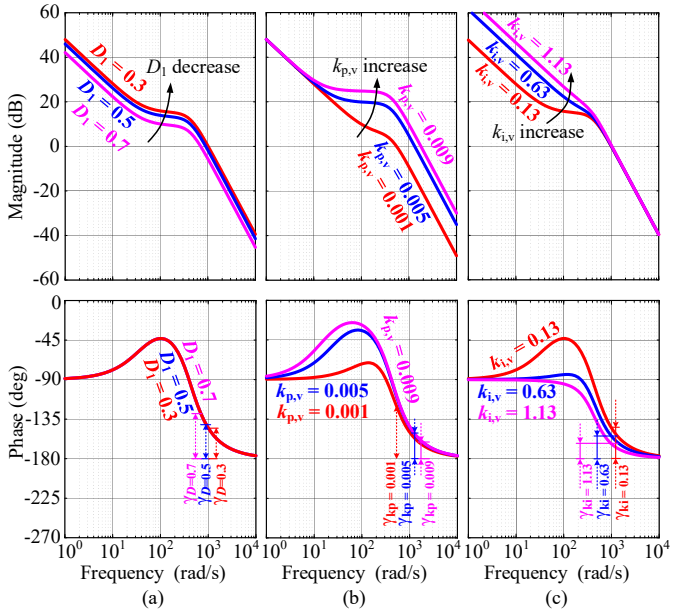


Fig. 14. Frequency responses of the open-loop system in fault tolerant operation for the reverse power flow: (a) when $k_{p,v}$ = 0.005, $k_{i,v}$ = 0.13, (b) when D_1 = 0.3, $k_{i,v}$ = 0.13, and (c) when D_1 = 0.3, $k_{p,v}$ = 0.003.

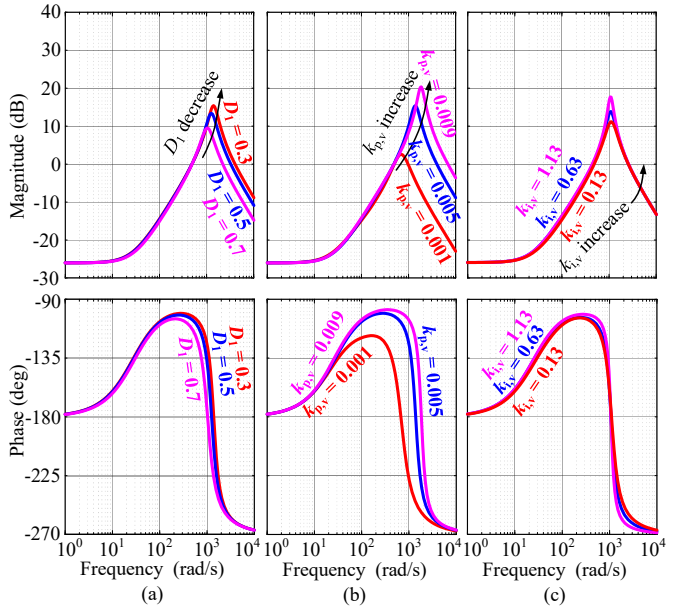


Fig. 15. Frequency responses of the closed-loop system in fault tolerant operation for the reverse power flow: (a) when $k_{p,v}$ = 0.005, $k_{i,v}$ = 0.13, (b) when D_1 = 0.3, $k_{i,v}$ = 0.13, and (c) when D_1 = 0.3, $k_{p,v}$ = 0.003.

sudden change of e_u will introduce harmonics near the resonant peak. Subsequently, the harmonics are amplified, resulting in large low-frequency oscillations as the envelope of the high-frequency current.

B. Reverse Power Flow (Buck Mode)

The frequency response of the open-loop system $G_{vol}(s)\cdot G_{ud1}(s)$ for the reverse power flow is shown in Fig. 14. As it can be seen in Fig. 14, the variation of D_1 only has a negligible impact on the frequency response of $G_{vol}(s)\cdot G_{ud1}(s)$. The increase of $k_{p,v}$ and $k_{i,v}$ leads to higher magnitudes of the open-loop system in the high and low frequency bands, respectively. When $k_{p,v}$ = 0.005, $k_{i,v}$ = 0.13, the cut-off frequency is around 1000 rad/s, and the phase margin γ is larger than 34° with D = 0.3 ~ 0.7. It means that the system is stable. Referring to Fig. 11, the frequency responses of $G_{ie,cls}(s)$ = $i_{r,avg}(s)$ / $e_u(s)$ for the reverse power flow case are given in Fig. 15. Similar to the forward power flow condition, $G_{ie,cls}(s)$ has an obvious peak. The peak moves to higher-frequency and becomes larger with the decrease of D_1 and increase of $k_{p,v}$ and $k_{i,v}$. However, the amplitude of the peak (e.g., 20.3 dB in Fig. 15(b) with $k_{p,v}$ = 0.009) is lower compared to that for the forward power flow (e.g., 36.5 dB in Fig. 13(b) with $k_{p,v}$ = 0.009). It indicates that the above-mentioned oscillation may not appear in the reverse power flow mode.

According to the above analysis, the low-frequency oscillation is apt to occur in the forward power flow case. To suppress this oscillation, a notch filter may be inserted in the feedback loop to attenuate the oscillations. However, since the resonant peak varies with the duty-cycle and the controller parameter $k_{p,v}$, it is not easy to select the central frequency of the notch filter. Moreover, as the DC capacitance is time-varying in DC distribution systems due to DC loading changes, the resonant frequency of L_r and C_{dc} is even difficult to determine. Therefore, the voltage single-loop control is not capable to suppress the low frequency oscillations during fault tolerant operation.

V. Proposed Dual-Loop Fault Tolerant Control Method

In order to address the above issues, a dual-loop fault tolerant control method is proposed in this section. Firstly, since there are many nonlinear elements in the model of the system, as shown in Fig. 10, a correction unit is introduced in the control loop, as shown in Fig. 16(a). By doing so, the trigonometric term $\sin d\pi/2$ in Fig. 10 is corrected as $\sin \pi/2\left(2/\pi \arcsin d_m\right) = d_m$. After the correction, the system can be described as

$$\begin{bmatrix} \dot{\hat{i}}_{r,avg} \\ \dot{\hat{u}}_o \end{bmatrix} = A_m\hat{x} + B_m\hat{u}_i + K_m\hat{d}_{2m}$$
$$= \begin{bmatrix} 0 & -\dfrac{8\sqrt{2}D_{2m}}{\pi^3 L_r} \\ \dfrac{D_{2m}}{C_{dc}} & -\dfrac{1}{R_L C_{dc}} \end{bmatrix} \begin{bmatrix} \hat{i}_{r,avg} \\ \hat{u}_o \end{bmatrix} + \begin{bmatrix} \dfrac{4\sqrt{2}}{\pi^3 L_r} \\ 0 \end{bmatrix} \hat{u}_i + \begin{bmatrix} -\dfrac{4\sqrt{2}U_i}{\pi^3 L_r D_{2m}} \\ \dfrac{U_i}{2R_L C_{dc} D_{2m}^2} \end{bmatrix} \hat{d}_{2m} \quad (12)$$

for the forward power flow. The transfer function of the system can be obtained as

$$\begin{bmatrix} G_{ird2}(s) \\ G_{ud2}(s) \end{bmatrix} = \frac{\begin{bmatrix} -\dfrac{4\sqrt{2}U_i}{\pi^3 L_r D_{2m}}\left(s + \dfrac{2}{R_L C_{dc}}\right) & \dfrac{U_i}{C_{dc}}\left[\dfrac{1}{2R_L D_{2m}}s - \dfrac{4\sqrt{2}}{\pi^3 L_r}\right] \end{bmatrix}^T}{s^2 + \left(\dfrac{1}{R_L C_{dc}}\right)s + \dfrac{8\sqrt{2}D_{2m}^2}{\pi^3 L_r C_{dc}}} \quad (13)$$

For the reverse power flow, the systems is described as

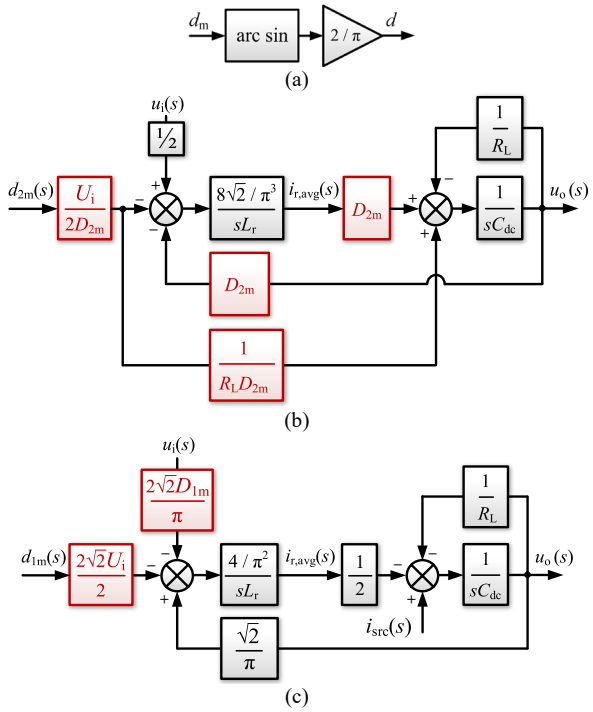


Fig. 16. Dynamic equivalent model after the nonlinearity correction: (a) correction unit, (b) modified block diagram for the forward power flow case, and (c) modified block diagram for the reverse power flow case.

$$\begin{bmatrix}\dot{\hat{i}}_{r,avg}\\ \dot{\hat{u}}_o\end{bmatrix}=\begin{bmatrix}0 & \frac{4\sqrt{2}}{\pi^3 L_r}\\ -\frac{1}{2C_{dc}} & -\frac{1}{R_L C_{dc}}\end{bmatrix}\begin{bmatrix}\hat{i}_{r,avg}\\ \hat{u}_o\end{bmatrix}+\begin{bmatrix}-\frac{8\sqrt{2}D_{2m}}{\pi^3 L_r} & 0\\ 0 & \frac{1}{C_{dc}}\end{bmatrix}\begin{bmatrix}\hat{u}_i\\ \hat{i}_{src}\end{bmatrix}+\begin{bmatrix}-\frac{8\sqrt{2}U_i}{\pi^3 L_r}\\ 0\end{bmatrix}\hat{d}_{1m} \quad (14)$$

The transfer function of the system can be obtained as

$$\begin{bmatrix}G_{ird1}(s)\\ G_{ud1}(s)\end{bmatrix}=\frac{-\frac{8\sqrt{2}U_i}{\pi^3 L_r}\begin{bmatrix}s+\frac{1}{R_L C_{dc}} & -\frac{1}{2C_{dc}}\end{bmatrix}^T}{s^2+\left(\frac{1}{R_L C_{dc}}\right)s+\frac{2\sqrt{2}}{\pi^3 L_r C_{dc}}} \quad (15)$$

According to (12) and (14), the state-space models of the modified system are presented in Fig. 16(b) and (c). As shown in Fig. 16, the nonlinear correction unit simplifies the model. For the reverse power flow, the proposed model is very similar to the conventional DC/DC buck converter, indicating that the single-voltage closed-loop control is sufficient to stabilize the system. However, for the forward power flow, the proposed model is very similar to the conventional DC/DC boost converter. It implies that the resonant frequency of the system is also duty-cycle-dependent, and the system is a non-minimum phase system. Therefore, the conventional single-voltage closed-loop control method cannot guarantee a good control performance.

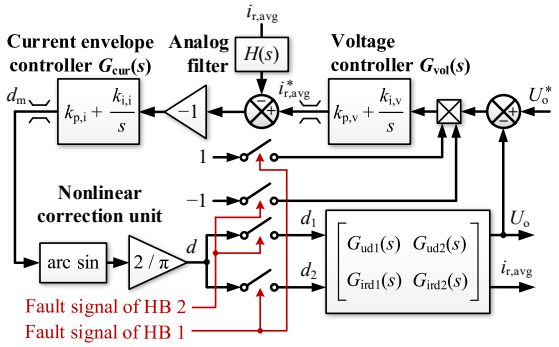


Fig. 17. Control diagram of the proposed dual-loop fault tolerant method.

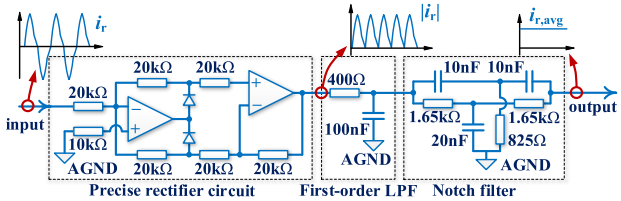


Fig. 18. Signal conditioning circuit to extract the absolute average current.

Since the voltage/current dual-loop control method is widely used in DC/DC boost converters, a cascaded dual-loop fault tolerant method is proposed. More specifically, the outer loop regulates the rectified DC voltage and the inner loop controls the envelope of the high-frequency current to suppress the oscillation. For the inner current envelope controller, the absolute average value of the inductor current $i_{r,avg}$, is employed as the control variable. With this, the entire control diagram can be obtained, as shown in Fig. 17, where $G_{cur}(s)$ represents the inner current envelope PI controller, and $k_{p,i}$ and $k_{i,i}$ are its proportional and integral gains.

To extract the absolute average current $i_{r,avg}$, a signal-conditioning circuit has been designed, as shown in Fig. 18. This circuit firstly transfers the high frequency current signal into its absolute value $|i_r|$, and through a first-order low-pass filter (LPF), the average value of $i_{r,avg}$ can be acquired. A notch filter is subsequently cascaded to eliminate the output ripples at the double-switching frequency, enhancing the quality of the output signal. It should be noted that the phase-lag introduced by this signal conditioning circuit is negligible. The amplitude-frequency characteristic of the notch filter is very sharp near the double switching frequency, and has negligible influence on the low frequency components. Therefore, the current envelope control loop can be designed with a high bandwidth. According to Fig. 18, the transfer function of the signal-conditioning circuit can be approximated by a first-order LPF, i.e., $H(s)\approx 1/\left(4\times10^{-5}s+1\right)$. Notably, there is no other additional hardware. The proposed method is very cost-effective.

A. Forward Power Flow

For the parameter design of the current controller, the open-loop Bode plots of the inner current loop can be used, as shown in Fig. 19. As it can be seen in Fig. 19(a), when $k_{p,i}$ = 0.008, $k_{i,i}$ = 5, the cut-off frequency of the inner loop

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2975348, IEEE Transactions on Power Electronics

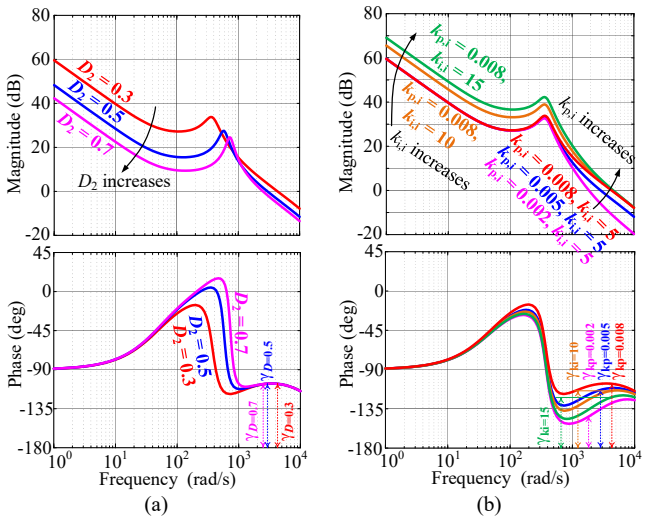


Fig. 19. Frequency responses of the current open-loop system for the forward power flow: (a) when $k_{p,i}$ = 0.008, $k_{i,i}$ = 5, and (b) when D_2 = 0.3, with varying $k_{p,v}$ and $k_{i,v}$.

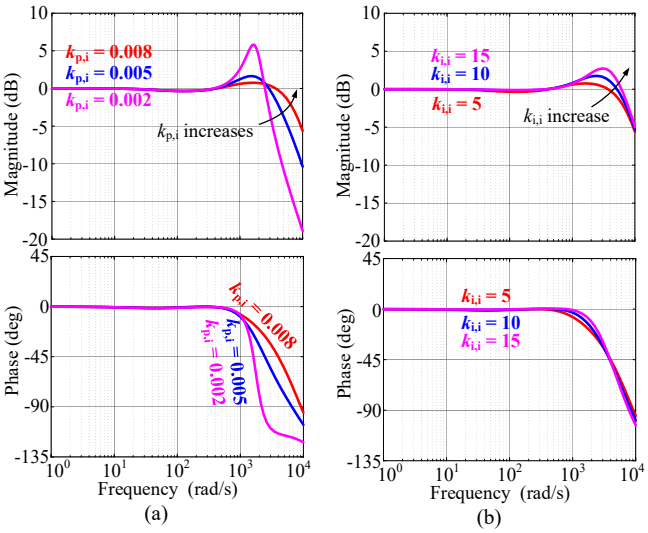


Fig. 20. Frequency responses of the current closed-loop system for the forward power flow: (a) when D_2 = 0.3, $k_{i,i}$ = 5, and (b) when D_2 = 0.3, $k_{p,i}$ = 0.008.

system is placed between 2000 ~ 5000 rad/s, and thus, the current control bandwidth is relatively high. The phase margin is 73° when D_2 = 0.7, which is sufficient to ensure the control stability. The increase of $k_{p,i}$ will lead to a higher bandwidth and a higher phase margin of the inner current loop, as shown in Fig. 19(b). However, the phase margin will drop if $k_{p,i}$ is too large, as the analog filter will introduce a pole in the high-frequency region. On the other hand, the increase of $k_{i,i}$ will raise the amplitude-frequency curve in the low-frequency region, bringing a better steady-state performance; at the same time, it moves the phase-frequency curve downward, and decreases the phase margin of the current loop.

Furthermore, the closed-loop Bode plots of the inner current loop are given in Fig. 20 when D_2 = 0.3. As shown in Fig. 20, when $k_{i,i}$ = 5, with the increase of $k_{p,i}$, the resonant peak can effectively be suppressed. On the other hand, when $k_{p,i}$ = 0.008,

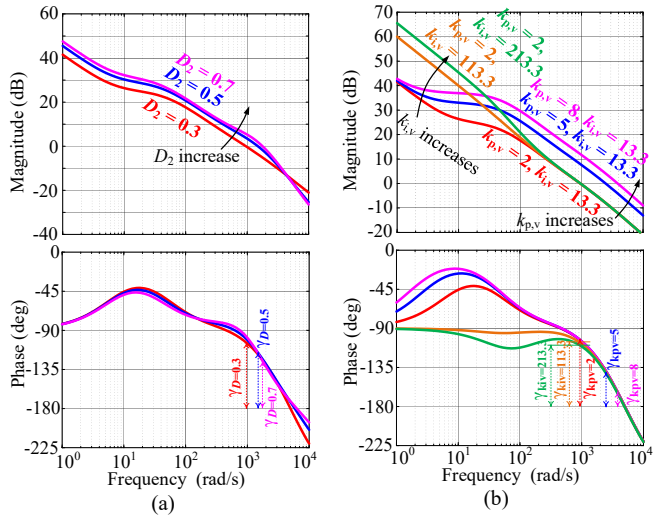


Fig. 21. Frequency responses of the voltage open-loop and current closed-loop system for the forward power flow: (a) when $k_{p,v}$ = 2, $k_{i,v}$ = 13.3, $k_{p,i}$ = 0.008, $k_{i,i}$ = 5, and (b) when D_2 = 0.3, $k_{p,i}$ = 0.008, $k_{i,i}$ = 5.

the increase of $k_{i,i}$ will slightly increase the resonant peaks of the current closed-loop system, while pushing the peaks to the higher frequency region. As discussed in the above, the parameters of the current loop can be properly tuned.

To tune the parameters of the voltage outer-loop controller, the frequency responses of the voltage open-loop and current closed-loop systems are shown in Fig. 21. As seen in Fig. 21(a), when $k_{p,v}$ = 2, $k_{i,v}$ = 13.3, $k_{p,i}$ = 0.008, $k_{i,i}$ = 5, the cut-off frequency of the voltage loop is around 1000 rad/s, with a phase margin larger than 54° under different static duty-cycles. The increase of $k_{p,v}$ and $k_{i,v}$ will enhance the dynamic and steady-state voltage control performances, respectively, but the phase margin will be reduced, as shown in Fig. 21(b). Compared to the voltage single-loop control, where either the phase margin or the control bandwidth should be compromised, the proposed dual-loop method can keep high control bandwidth and a large phase margin. Therefore, with the proposed method, fast fault tolerant dynamics, high stability and suppression of the low-frequency oscillations can be achieved.

B. Reverse Power Flow.

The frequency responses for the reverse power flow are shown in Fig. 22. As it can be seen in Fig. 22(a), the cut-off frequencies of the inner loop system under different control parameters are between 1500 ~ 5000 rad/s, with a phase margin larger than 55°, indicating that the current loop is always stable. The increase of $k_{p,i}$ and decrease of $k_{i,i}$ will lead to a higher phase margin. However, if if $k_{p,i}$ is too high, the phase margin can be decreased owing to the phase-lag introduced by the analog filter. The resonant peak of the closed-loop current control can be effectively suppressed, as shown in Fig. 22(b) and (c). It is further implied in Fig. 22(d) that the voltage loop is stable. When $k_{p,v}$ = 2, $k_{i,v}$ = 13.3, $k_{p,i}$ = 0.008, $k_{i,i}$ = 5, the cut-off frequency of the voltage loop is set around 1000 rad/s, with a phase margin of 82°. Therefore, for the reverse power flow, the stability of the system can also be guaranteed by the proposed dual-loop control method.

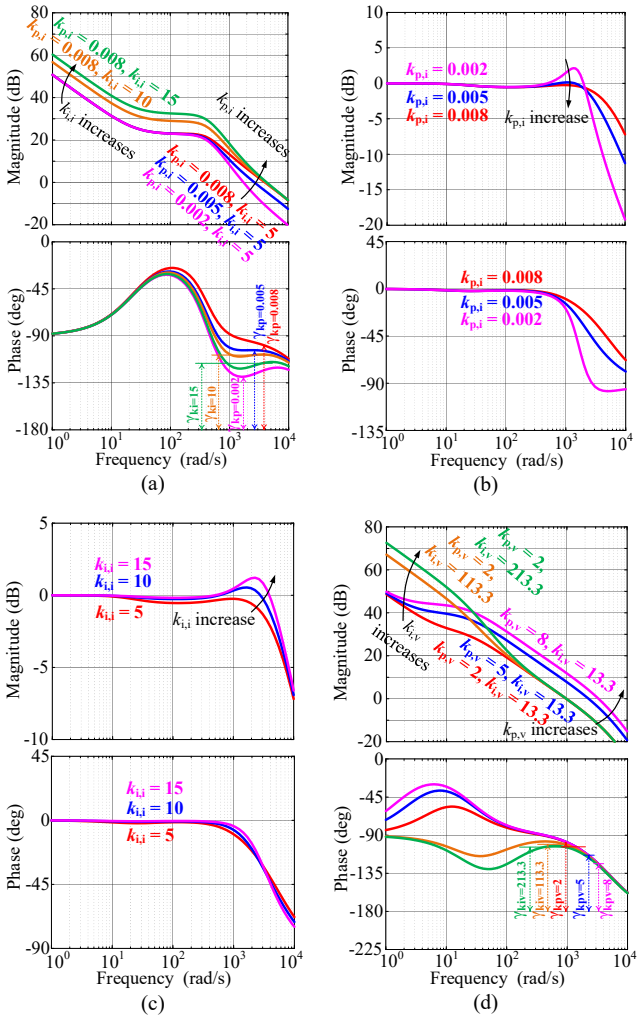


Fig. 22. Frequency responses of the system for the reverse power flow: (a) Bode plots of the current open-loop system, (b) Bode plots of the current closed-loop system when $k_{i,i}$ = 5, (c) Bode plots of the current closed-loop system when $k_{p,i}$ = 0.008, and (d) Bode plots of the voltage open-loop and current closed-loop system.

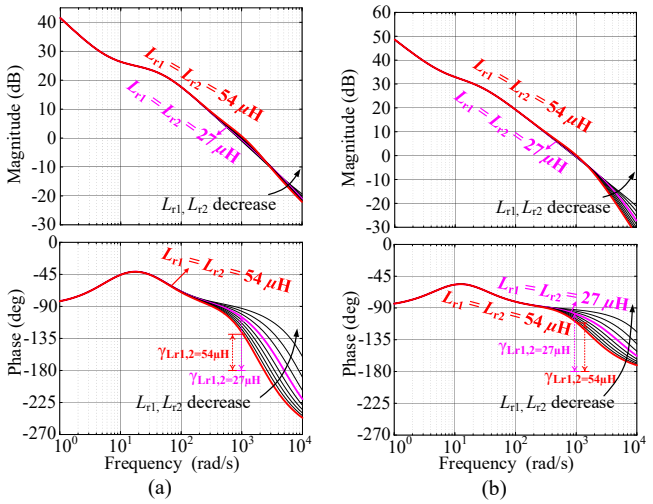


Fig. 23. Frequency responses of the voltage open-loop and current closed-loop system when L_{r1} and L_{r2} varies between 10.8 μH to 54 μH: (a) for the forward power flow, and (b) for the reverse power flow.

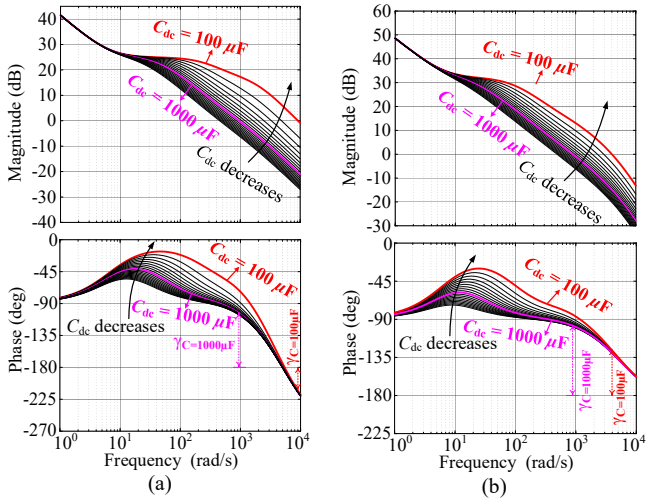


Fig. 24. Frequency responses of the voltage open-loop and current closed-loop system when C_{dc} varies between 100 μF to 1000 μF: (a) for the forward power flow, and (b) for the reverse power flow.

VI. Parameter Uncertainty Analysis

In DC distribution systems, the DC loads are always time-variant. To validate the stability of the system under parameter uncertainties, the parameter uncertainty analysis is detailed in this section. For the SRDAB, three parameter uncertainties cases are considered: resonant inductance L_r, DC capacitance C_{dc}, and DC load R_L.

Firstly, in practice, the value of resonant inductance is known to determine the switching frequency. Its uncertainties should be within a small range, e.g., ±10% for the worst case. Considering an even larger range of inductance variations, the control system responses are shown in Fig. 23. As it can be seen in Fig. 23, the cut-off frequencies are almost constant for different L_r values, while the phase margins slightly decrease from 88° to 49° for the forward power flow, and 88° to 69° for the reverse power flow when L_r increases from 21.6 μH to 108 μH (−60% ~ 100%). Thus, it can be confirmed by Fig. 23 that the resonance inductance uncertainties have negligible impact on the system stability.

Additionally, due to load variations, the DC capacitance may change. Fig. 24 shows the frequency response of the system when C_{dc} varies between 100 μF to 2000 μF (−90% ~ +100% of the rated). It can be seen in Fig. 24 that the phase margins are not changed, but the cut-off frequency increases with the decrease of C_{dc}. According to Fig. 24, the critical value of the DC capacitance is about 100 μF. In this condition, the phase margin is −36° for the forward power flow, and 53° for the reverse power flow. Therefore, large DC capacitors should be used in the SRDAB to ensure its fault-tolerant capabilities. This is practical in the DC distribution systems, as larger DC capacitance will also help to smooth the voltage fluctuations.

Moreover, when the load changes, the system stability may be different. Fig. 25 presents the frequency responses of the system when R_L varies between 10 Ω to 80 Ω (−75% ~ +100%

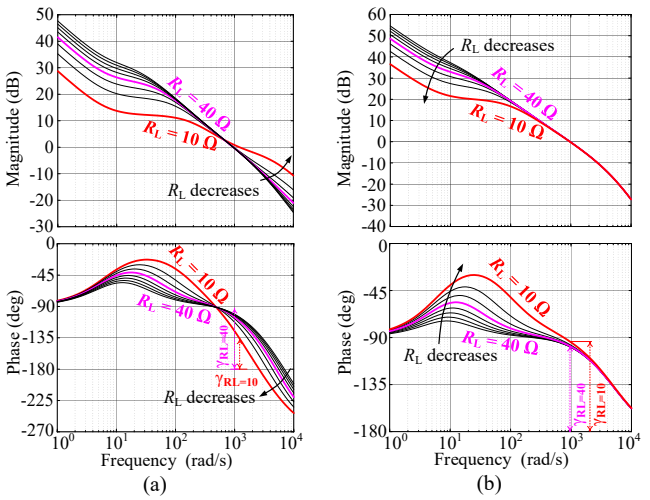


Fig. 25. Frequency responses of the voltage open-loop and current closed-loop system when R_L varies between 10 Ω to 80Ω: (a) for the forward power flow, and (b) for the reverse power flow.

of the rated, and load power varies between 7 kW to 56 kW). As it can be seen in Fig. 25(a), the phase margin decreases with the increase of load power for the forward power flow. In contrast, as shown in Fig. 25(b), the load variation has negligible impact on the phase margin in the reverse power flow mode. However, since the power of the 10-Ω load is already 4 times larger than the nominal, the over-current protection should be triggered for even larger load condition. Therefore, if the load is within the nominal power range of the SRDAB, the proposed controller performs robustly.

VII. Simulation and Experimental Results

To validate the effectiveness of the proposed control method, simulation and experimental tests are performed referring to Fig. 1.

A. Simulation Results

1) Test 1: To illustrate the low-frequency oscillations by the resonant inductors and the rectifier DC capacitors for the forward power flow, the voltage single-loop fault tolerant method using a voltage single-loop control in [23] was applied, and the simulation results are provided in Fig. 26. The duty-cycle threshold d_{th} is set as 0.1, and $k_{p,v}$ = 0.009, $k_{i,v}$ = 0.13. At t = 0.15 s, the open-circuit fault of S_1 happens. As shown in Fig. 26, the rectified DC voltage is quickly maintained and slowly restores to its nominal value. The voltage drop is only 70 V (9.3% voltage drop). The resonant process is interrupted by the duty-cycle regulation and the duty-cycle of the rectifier-side output voltage is around 1/3 (as in Stage II in Fig. 4), as shown in Fig. 26. The transient lasts for 88 ms with small low-frequency fluctuations in the DC voltage and DC current, and then, the SRDAB enters into Stage III and reconfigures to a half-bridge system. All semiconductors commutate at zero-current intervals during Stage III, as shown in the right-bottom of Fig. 26. The output current I_{dc2} is kept around 18 A during the entire process,

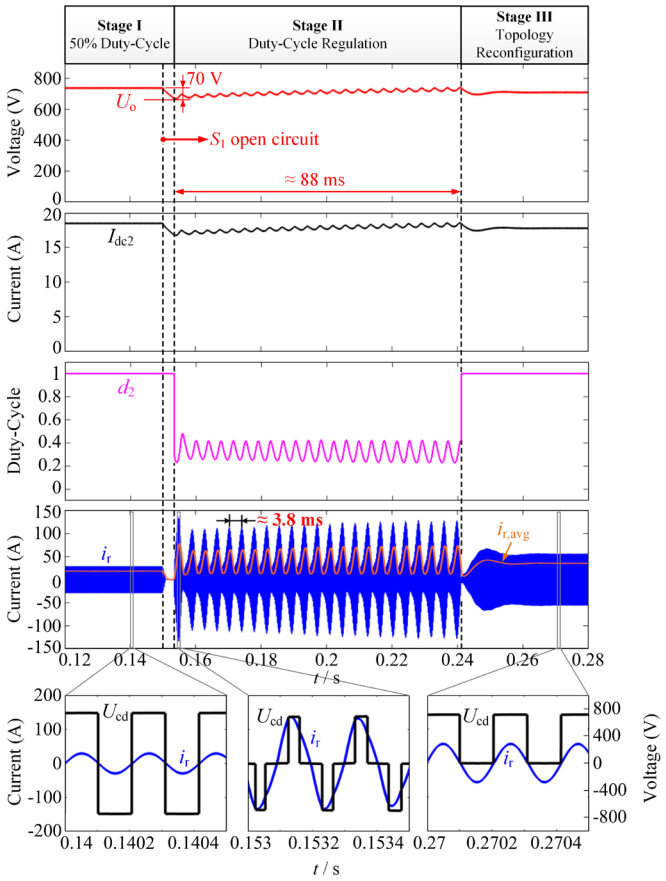


Fig. 26. Control performance of the voltage single-loop fault tolerant method for the forward power flow of SRDAB when $k_{p,v}$ = 0.009, $k_{i,v}$ = 0.13.

indicating that the output power of the converter is approximately constant. The fault tolerant control is achieved.

However, during the duty-cycle regulation period, a remarkable low frequency oscillation at about 263 Hz as the envelope of the high frequency current appears, as shown in Fig. 26. This oscillation frequency is highly correspondent with the Bode plot in Fig. 13(b), when $k_{p,v}$ = 0.009 and D_2 = 0.3, where the resonant frequency is around 1650 rad/s (≈ 262.6 Hz). The maximum peak current reaches 133 A, as shown in Fig. 26, which is 4.4 times more than the nominal current. The envelope of the high frequency current keeps oscillating until the fault tolerant control proceeds to Stage III. Although the output voltage is stable with small low frequency fluctuations during the fault tolerant operation, the current oscillation may trigger the over-current protection, leading to fault tolerant failures for the SRDAB converter in DC distribution systems.

2) Test 2: To validate the correctness of the previous analysis, simulation results regarding two more cases when D_2 ≈ 0.5 and 0.7 are given in Fig. 27. In this simulation, $k_{p,v}$ = 0.005 and $k_{i,v}$ = 0.13, and the DC reference voltage jumps from 750 V to 500 V (D_2 ≈ 0.5 in the steady state) at 0.5 s and 400 V (D_2 ≈ 0.7 in the steady state) at 0.8 s. As it can be seen, when the reference voltage is 750 V, there are remarkable oscillations at about 208 Hz as the output voltage and the envelope of the high-frequency current. When the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2975348, IEEE Transactions on Power Electronics

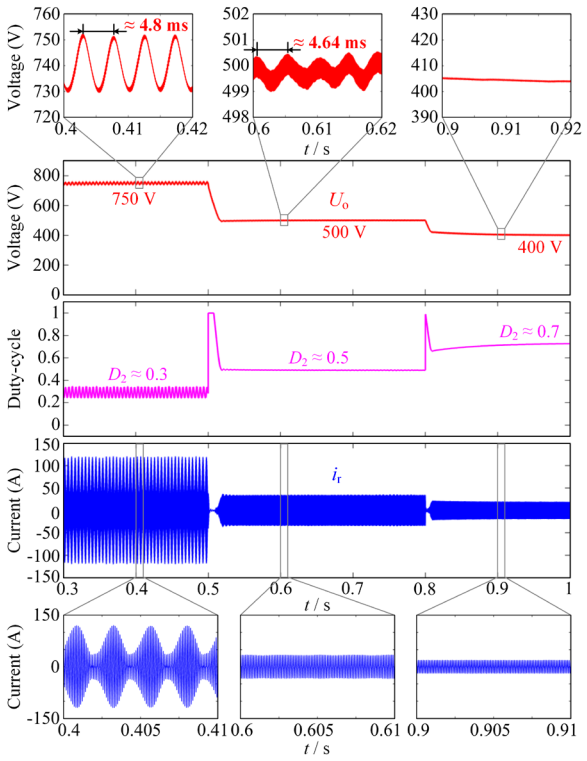


Fig. 27. Control performance of the voltage single-loop fault tolerant method for the SRDAB with different static duty-cycle D for the forward power flow.

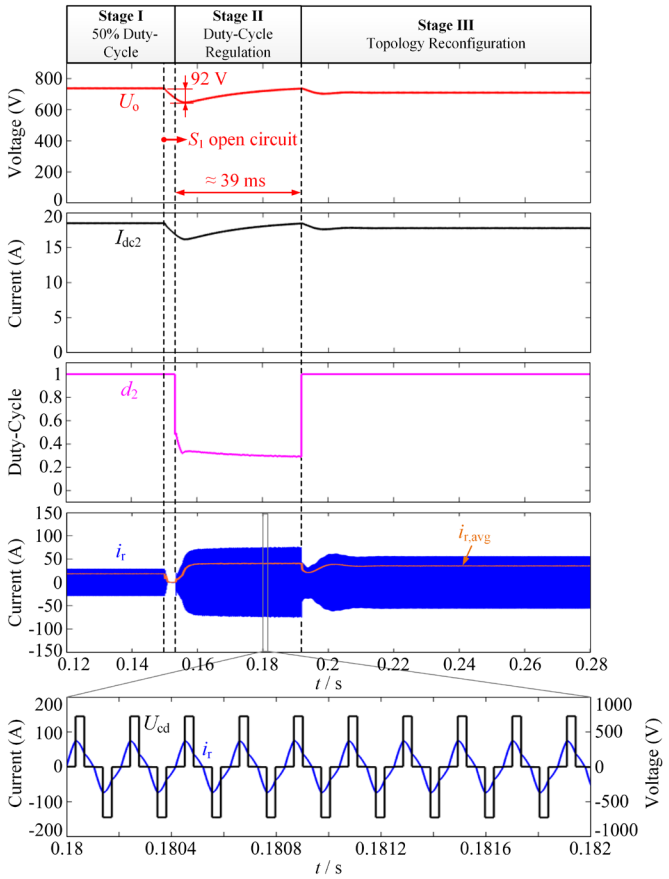


Fig. 28. Control performance of the proposed dual-loop fault tolerant method for the forward power flow of SRDAB.

reference voltage is 500 V, the output voltage oscillate at a frequency of 216 Hz with a very small amplitude of 1 V, and when the reference voltage is 400 V, no oscillation can be observed in the output voltage. For the last two cases, there are no obvious oscillations as the envelope of the high-frequency current. This phenomenon is in accordance with the bode plot in Fig. 13(a), where it has been shown that the resonant peak becomes higher in amplitude with the decrease of D_2, being about 4.9 dB (1.76 times gain) at 186 Hz, 11.5 dB (3.76 times gain) at 204 Hz and 20.9 dB (11.1 times gain) at 196 Hz for $D_2 = 0.7$, 0.5 and 0.3, respectively.

3) Test 3: Simulation results of the proposed dual-loop fault tolerant control method are presented in Fig. 28 for the forward power flow. The control parameters are $k_{p,v} = 2$, $k_{i,v} = 13.3$, $k_{p,i} = 0.008$, $k_{i,i} = 5$. As it can be seen in Fig. 28, after the open-circuit fault of S_1 occurs at $t = 0.15$ s, the output DC voltage maintains and restores to its nominal value with a maximum voltage drop of 92 V during the transient period of 39 ms. In contrast to the results in Test 1, the envelope of the high-frequency current is kept flat and stable, with a peak current of 76 A (i.e., only 2.5 times of the nominal). During the duty-cycle regulation period, the regulated duty-cycle d_2 is stable around 1/3, and there are no fluctuations in the output DC voltage. Thus, by implementing the proposed method, the low frequency oscillation can be effectively suppressed, ensuring fast and stable fault tolerant operation.

4) Test 4: To show the fault tolerant control performance of the proposed dual-loop method under parameter uncertainties, simulation results regarding C_{dc}, R_L, and L_r uncertainties are shown in Figs. 29, 30 and 31.

a) C_{dc} uncertainty: According to Fig. 24(a), the decrease of C_{dc} will decrease the phase-margin of the system for the forward power flow. Therefore, a −50% variation case of C_{dc} (C_{dc} = 500 μF) is firstly simulated, and the results are shown in Fig. 29(a), where it can be observed that the system is stable after the S_1-open-circuit fault. For lower C_{dc} values, simulation results are provided in Fig. 29(b) when C_{dc} = 100 μF for the forward power flow. As it can be seen, there are remarkable oscillations on the output voltage and high-frequency current, indicating the system becomes unstable with the fault tolerant control. However, for the reverse power flow, the system remains stable when C_{dc} = 100 μF, as shown in Fig. 29(c). These results are in accordance with Fig. 24, where the phase-margin of the open-loop system is positive for C_{dc} = 500 μF, and negative for C_{dc} = 100 μF, while the system can still be stable for the reverse power flow when C_{dc} = 100 μF. Besides, the transient voltage variation is increased to 210 V and 263 V, as shown in Fig. 29(b) and (c), which means that the decrease of C_{dc} will also bring higher voltage variations at the beginning of the fault tolerant control. Thus, it is suggested equipping larger DC capacitors for the SRDAB converter to ensure a good fault tolerant performance. However, it can be confirmed that the system performs robustly for DC capacitance uncertainties.

b) R_L uncertainties: Firstly, for the forward power flow case, a load step change within the nominal power range of the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2020.2975348, IEEE Transactions on Power Electronics

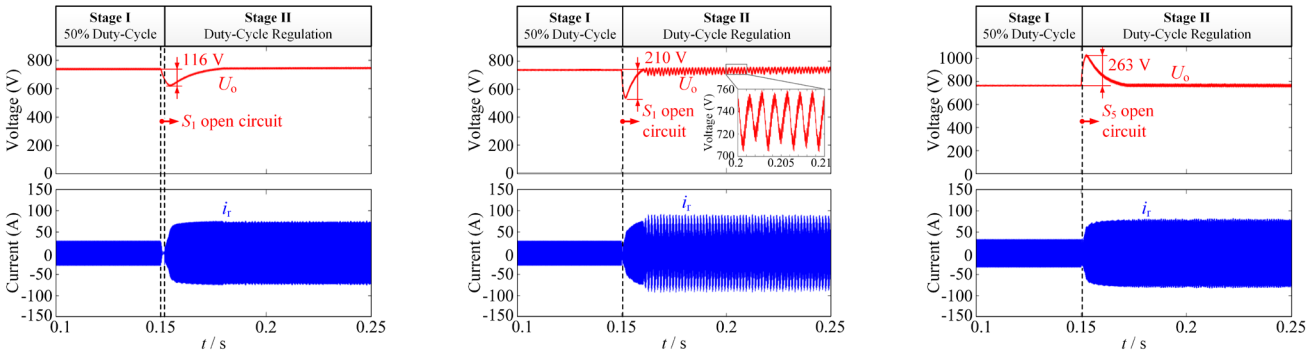


Fig. 29. Control performance of the proposed dual-loop fault tolerant method for the SRDAB under DC capacitance uncertainties: (a) C_{dc} = 500 μF for the forward power flow, (b) C_{dc} = 100 μF for the forward power flow, and (c) C_{dc} = 100 μF for the reverse power flow.

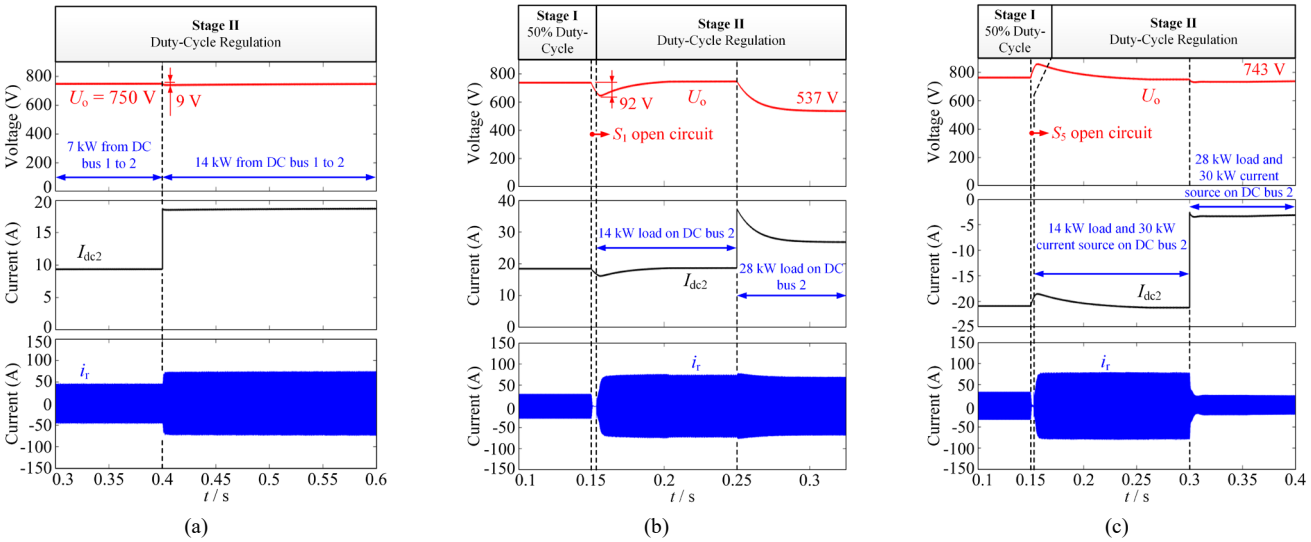


Fig. 30. Control performance of the proposed dual-loop fault tolerant method for the SRDAB under DC load uncertainties: (a) R_L changes from 80 Ω to 40 Ω for the forward power flow, (b) R_L changes from 40 Ω to 20 Ω for the reverse power flow, and (c) R_L changes from 40 Ω to 20 Ω for the forward power flow.

SRDAB is simulated, and the results are shown in Fig. 30(a), where R_L jumps from 80 Ω (7 kW) to 40 Ω (14 kW) at 0.4s. As shown in Fig. 30(a), the transient voltage drop is only 9 V (1.2%U_N) and there are no current surge on the output DC current I_{dc2} and the high-frequency current. The system performs very stable against load changes. For higher load power variation, simulation results where R_L jumps from 40 Ω to 20 Ω for the forward and reverse power flow are provided in Fig. 30(b) and (c), respectively. As shown in Fig. 30(b), the voltage of DC bus 2 drops to 537 V after the load change, and the amplitude of the high-frequency current is restricted within ±80 A all the time. This is because when the load power is beyond the maximum allowable value of the SRDAB, the output of the voltage controller will be saturated to avoid triggering the over-current protection. Therefore, although it has been discussed previously that higher power of load may destabilize the system, it is not possible to happen in practice, owing to the direct control of the current envelope. The output power can thus be restricted to prevent the system from entering the unstable region.

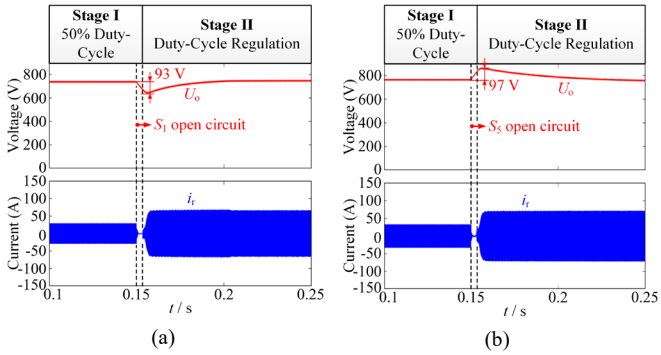


Fig. 31. Control performance of the proposed dual-loop fault tolerant method for the SRDAB under resonant inductance when L_{r1} = L_{r2} = 0.54 μH: (a) for the forward power flow, and (b) for the reverse power flow.

For the reverse power flow case in Fig. 30(c), it can be seen that the system is very stable when the load power jumps from 16 kW to 2 kW. Therefore, the system performs a good stability under load uncertainties.

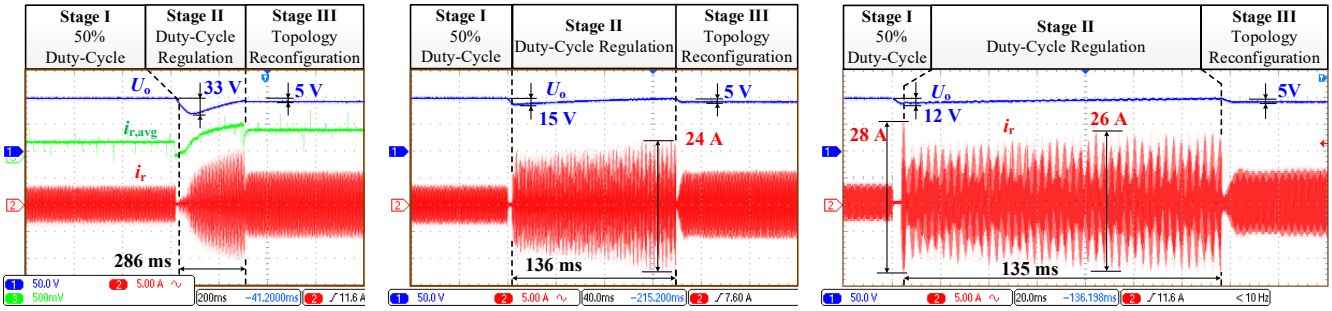


Fig. 32. Performance (experimental tests) of the SRDAB with the conventional voltage-single-loop method (U_o [50 V/div]: the output DC voltage; i_r [5 A/div]: the high frequency current; $i_{r,avg}$ [10 A/div]: the extracted current envelope from the analog circuit): (a) when $k_{p,v}$ = 0.001, $k_{i,v}$ = 0.03 (time [200 ms/div]), (b) when $k_{p,v}$ = 0.006, $k_{i,v}$ = 0.13 (time [40 ms/div]), and (c) when $k_{p,v}$ = 0.009, $k_{i,v}$ = 0.13 (time [20 ms/div]).

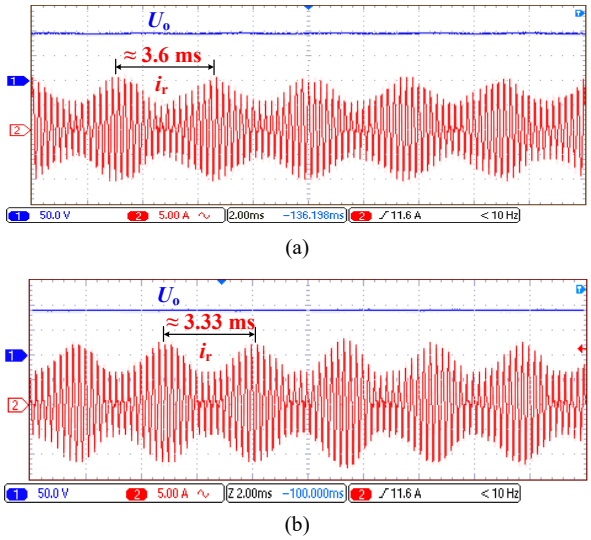


Fig. 33. Zoomed-in experimental results of Fig. 32 during the duty-cycle regulation period (U_o [50 V/div]: the output DC voltage; i_r [5 A/div]: the high frequency current; time [2 ms/div]): (a) zoomed-in plot of Fig. 32(b), and (b) zoomed-in plot of Fig. 32(c).

c) L_r uncertainties: as discussed previously, the phase margin of the system is decreased with the increase of L_r. Therefore, simulations for +50%-L_r variations (L_r = 108 μH, and in order to keep constant switching frequency, C_r = 1 μF) were conducted and the results are shown in Fig. 31(a) and (b). As shown in Fig. 31, the fault tolerant process is stable. Therefore, the system performs robustly under L_r uncertainties.

B. Experimental Results

To further validate the proposed method, experimental tests were performed on a downscaled 1-kW SRDAB prototype. The parameters of the experimental setup are shown in Table I. The control system was built with a TMS320F28335 digital signal processor and an EP4CE10 FPGA. The Mitsubishi PM50B4LA060 IPM was adopted to assemble the SRDAB interfacing converter. One DH1716-A programmable DC source was used as the input DC bus, and another one was employed as the DC current source on DC bus 2. The signal conditioning circuit is the same as that in Fig. 18. The experiments were conducted for both forward and reverse power flow.

1) Forward Power Flow: Firstly, the voltage single-loop fault tolerant method was tested under different control parameters. The experimental results are shown in Fig. 32, where $k_{p,v}$ = 0.001, $k_{i,v}$ = 0.065 for Fig. 32(a), $k_{p,v}$ = 0.006, $k_{i,v}$ = 0.13 for Fig. 32(b), and $k_{p,v}$ = 0.009, $k_{i,v}$ = 0.13 for Fig. 32(c). As shown in Fig. 32, at the beginning of the test, the output DC voltage was 96 V. The 4-V voltage drop was induced by the parasitic resistance and the deviation between the switching frequency and the actual series resonant frequency of the resonant tank [23]. Then, one switch in the H-bridge 1 was in open-circuit fault. As shown in Fig. 32(a), the output DC voltage restores to its nominal value after 286 ms, and then H-bridge 2 was reconfigured to be a half-bridge and operates in the open-loop mode. The extra 5-V voltage drop is because that the reconfigured half-bridge SRDAB has a larger voltage drop on the series parasitic resistance [23]. Although there are no oscillation as the envelope of the high-frequency current, the transient performance was sacrificed. The voltage drop during the fault tolerant operation is 33 V, which will highly affect the power supply quality of DC bus 2.

For the experimental results with increased $k_{p,v}$ and $k_{i,v}$ shown in Fig. 32(b), the output DC voltage was maintained at its output value with a voltage drop of only 15 V. When the open-circuit fault was identified within 136 ms, H-bridge 2 was reconfigured to be a half bridge. Although the fault tolerant control performance was improved with much lower voltage drop and shorter transient period compared with the Fig. 32(a), there are large oscillations with the frequency being about 278 Hz, as the envelope of the high-frequency current during the duty-cycle regulation period (fault tolerant operation), as shown in the zoomed-in plot in Fig. 33(a). The peak-to-peak value of the oscillations is measured to be 24 A, which is 3.4 times larger than the nominal current. This may trigger the system overcurrent protection and lead to fault tolerant failure.

In the experimental result shown in Fig. 32(c), a larger $k_{p,v}$ was tried. Even if the transient voltage drop is further reduced to 12 V, nevertheless, the oscillations as the envelope of the high-frequency current were increased, with the peak-to-peak value of the oscillations being 26 A, which is 3.7 times larger than the nominal current. Moreover, during the transition to

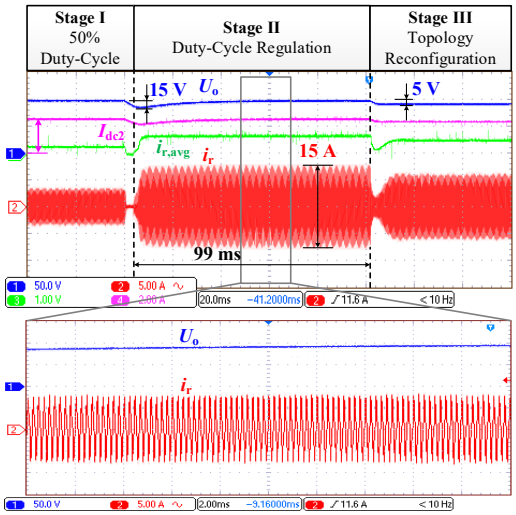


Fig. 34. Performance (experimental tests) of the SRDAB with the the proposed dual-loop method (U_o [50 V/div]: the output DC voltage; i_r [5 A/div]: the high frequency current of the H-bridge 1; $i_{r,avg}$ [20 A/div]: the extracted current envelope from the analog circuit; time – top [20 ms/div], time – bottom [2 ms/div]).

the fault tolerant operation, e.g., in the beginning of the fault tolerant control, the peak-to-peak value reaches 28 A, which is four times larger than the nominal current. The system will risk higher danger in triggering the overcurrent protection. Besides, the oscillation frequency was also increased to about 300 Hz because of larger $k_{p,v}$, as shown in the zoomed-in plot in Fig. 33(b). This is in accordance with the Bode plot analysis in Section IV. Therefore, it can be confirmed that the voltage single-loop method cannot have a satisfying fault tolerant control performance. Even if the oscillation can be suppressed by lower $k_{p,v}$ and $k_{i,v}$, higher voltage drop should be compromised. With larger $k_{p,v}$ and $k_{i,v}$, the transient voltage performance can be improved, but the oscillation will occur. In this condition, The SRDAB may fail to ride through the open-circuit fault.

The proposed dual-loop control method is then applied to the SRDAB system. The corresponding experimental results are shown in Fig. 34. In this case, the control parameters are $k_{p,v}$ = 2, $k_{i,v}$ = 13.3, $k_{p,i}$ = 0.008, $k_{i,i}$ = 5. As it is shown in Fig. 34, the output DC voltage can also be maintained, with a maximum voltage drop of 15 V for a short period. Different from the experimental results in Fig. 32(b) and (c), the high-frequency current envelope becomes flat and stable. That is, there are no low-frequency oscillations in the current. The peak-to-peak current is reduced to 15 A, being 2.1 times larger than the nominal current. The largest voltage drop is 15 V and the transient time for the duty-cycle regulation is 99 ms, which is slightly larger and shorter than the experimental results in Fig. 32(c), respectively. It can be explained that the saw-toothed edge in the waveform of the high-frequency current is caused by the poor resolution of the oscilloscope. The zoomed-in waveform and the current envelope $i_{r,avg}$ measured from the analog circuit illustrate that there are no oscillations. The output DC current I_{dc2} was also slightly reduced after the fault due to the additional voltage drop, but the output power

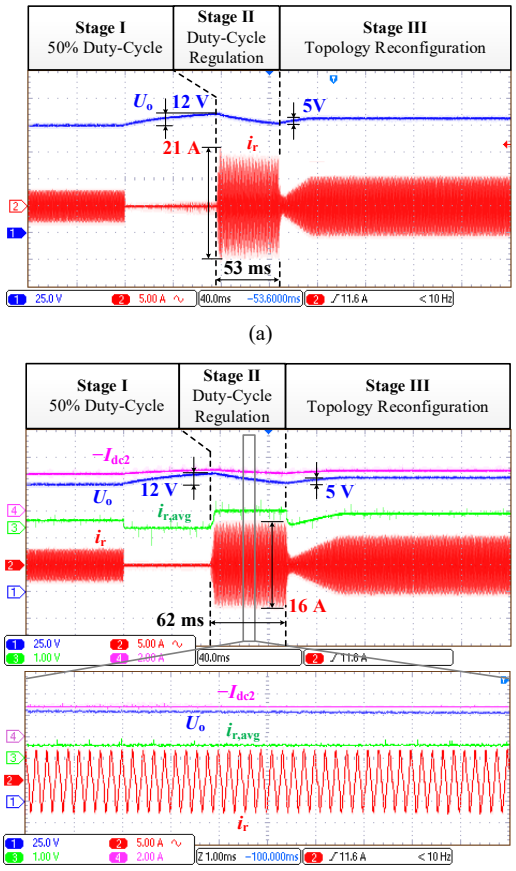


Fig. 35. Performance (experimental tests) of the SRDAB with the two fault tolerant methods (U_o [25 V/div]: the output DC voltage; i_r [5 A/div]: the high frequency current of the H-bridge 1; $i_{r,avg}$ [20 A/div]: the extracted current envelope from the analog circuit): (a) the voltage single-loop method (time [40 ms/div]) and (b) the proposed dual-loop method (time – top [40 ms/div], time – bottom [1 ms/div]).

of the converter is still approximately the same with the pre-fault condition. Therefore, the proposed dual-loop control method can effectively suppress the low-frequency oscillation induced by the resonant inductors and the DC capacitors under fault tolerant operation, as analyzed in the previous sections.

2) Reverse Power Flow: To perform the fault tolerant experiments for the reverse power flow, a 5-A DC current source was interfaced to DC bus 2. Firstly, the experimental results of the voltage single-loop fault tolerant method is shown in Fig. 35(a), where $k_{p,v}$ = 0.009 and $k_{i,v}$ = 0.13. As can be seen, the voltage of DC bus 2 was maintained after the one-switch open-circuit fault in H-bridge 2. The duty-cycle regulation period lasted for 53 ms with a maximum voltage rise of 12 V, and then the H-bridge 1 is reconfigured to a half bridge. Different from the forward power flow case, in the reverse power flow case, no obvious oscillations can be observed on the envelope of the high-frequency current. It means that the voltage single-loop fault tolerant method is capable to ensure the fast and stable fault tolerant operation of the SRDAB converter. However, an over-shooting can still be observed at the beginning of the fault tolerant control, being about 21 A, which is three times larger than the nominal

current. This current over-shooting may increase the potential risk of triggering the over-current protection.

To validate the effectiveness of the proposed dual-loop method for the reverse power flow, experimental results are shown in Fig. 35(b). As can be observed, the transient period is 62 ms with the maximum voltage rise of 12 V, and then the H-bridge 1 is reconfigured to a half-bridge. In this condition, the envelope of the high-frequency current is stable, which can be affirmed by the zoomed-in plot and the waveform of $i_{r,avg}$ measured from the analog circuit. Comparing to the last case, the amplitude of the high-frequency current is reduced to 16 A, being only 2.3 times higher than the nominal current. The waveform of the output current $-I_{dc2}$ shows the power delivered by the SRDAB converter is approximately the same before and after the fault tolerant control. Therefore, although the low-frequency oscillation does not occur in the reverse power flow case, the proposed dual-loop fault tolerant method can still be adopted to control the current within the permitted range, leading to lower risk of fault tolerant failure.

VIII. Conclusion

Low-frequency oscillations may appear as the envelope of the high-frequency current in the SRDAB during fault-toleration operation, when the voltage single-loop control is adopted. The mechanism of the low-frequency oscillations was explored in this paper through the detailed small signal models. More importantly, a dual-loop fault-tolerant control strategy was proposed for the SRDAB to suppress the low-frequency oscillations. The effectiveness of the proposed method lies that an outer loop is used to regulate the DC voltage, while the envelope of the high-frequency current is controlled through the inner loop. Simulation and experimental tests have been provided, which validated the performance of the proposed fault-tolerant control for the SRDAB in terms of easy implementation, high robustness, fast dynamics, and effective suppression of the oscillations.

References

[1] F. Blaabjerg, Y. Yang, D. Yang, and X. Wang, "Distributed power-generation systems and protection," *Proc. IEEE*, vol. 105, no. 7, pp. 1311–1331, Jul. 2017.

[2] J. E. Huber and J. W. Kolar, "Solid-state transformers: on the origins and evolution of key concepts," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19-28, Sept. 2016.

[3] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. F. Costa, and Z. Zou, "The smart transformer: impact on the electric grid and technology challenges," *IEEE Ind. Electron. Mag.*, vol. 10, no. 2, pp. 46-58, Jun. 2016.

[4] Y. Tian, P. C. Loh, F. Deng, Z. Chen, X. Sun, and Y. Hu, "Impedance coordinative control for cascaded converter in bidirectional application," *IEEE Trans. Ind. Appl*., vol. 52, no. 5, pp. 4084-4095, Sept./Oct. 2016..

[5] L. F. Costa, G. Buticchi, and M. Liserre, "Quad-active-bridge DC–DC converter as cross-link for medium-voltage modular inverters," *IEEE Trans. Ind. Appl*., vol. 53, no. 2, pp. 1243-1253, Mar./Apr. 2017.

[6] H. Mahmood, D. Michaelson, and J. Jiang, "A power management strategy for PV/battery hybrid systems in islanded microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 4, pp. 870-882, Dec. 2014.

[7] J. E. Huber, J. Miniböck, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle DCM series resonant converters," *IEEE Trans. Power Electron*., vol. 33, no. 1, pp. 4-7, Jan. 2018.

[8] J. Sun, L. Yuan, Q. Gu, R. Duan, Z. Lu, and Z. Zhao, "Design-oriented comprehensive time-domain model for CLLC class isolated bidirectional DC-DC converter for various operation modes," *IEEE Trans. Power Electron*., DOI: 10.1109/TPEL.2019.2938312

[9] G. Ortiz, M. G. Leibl, J. E. Huber, and J. W. Kolar, "Design and experimental testing of a resonant DC–DC converter for solid-state transformers," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7534-7542, Oct. 2017.

[10] L. Costa, G. Buticchi, and M. Liserre, "A fault-tolerant series-resonant DC–DC converter," *IEEE Trans. Power Electron*., vol. 32, no. 2, pp. 900-905, Feb. 2017.

[11] L. Costa, G. Buticchi, and M. Liserre, "Bidirectional series-resonant DC-DC converter with fault-tolerance capability for smart transformer," in *Proc. IEEE Energy Conversion Congr. and Expo. (ECCE)*, Milwaukee, WI, 2016, pp. 1-7.

[12] L. F. Costa, G. Buticchi, and M. Liserre, "A family of series-resonant DC–DC converter with fault-tolerance capability," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 335-344, Jan./Feb. 2018.

[13] L. Corradini, D. Seltzer, D. Bloomquist, R. Zane, D. Maksimović, and B. Jacobson, "Minimum current operation of bidirectional dual-bridge series resonant DC/DC converters," *IEEE Trans. Power Electron*., vol. 27, no. 7, pp. 3266-3276, Jul. 2012.

[14] F. M. Ibanez, J. M. Echeverria, J. Vadillo, and L. Fontan, "A step-up bidirectional series resonant DC/DC converter using a continuous current mode," *IEEE Trans. Power Electron*., vol. 30, no. 3, pp. 1393-1402, Mar. 2015.

[15] F. Ibanez, J. M. Echeverria, J. Vadillo, and L. Fontan, "Frequency response analysis for bidirectional series resonant DC/DC converter in discontinuous mode," *IET Power Electron*., vol. 7, no. 9, pp. 2374-2386, Sept. 2014.

[16] U. Choi, F. Blaabjerg, and K. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron*., vol. 30, no. 5, pp. 2517-2533, May 2015.

[17] U. Choi, F. Blaabjerg, and K. Lee, "Reliability improvement of a T-type three-level inverter with fault-tolerant control strategy," *IEEE Trans. Power Electron*., vol. 30, no. 5, pp. 2660-2673, May 2015.

[18] F. Wu, J. Zhao, Y. Liu, D. Zhou, and H. Luo, "Primary source inductive energy analysis based real-time multiple open-circuit fault diagnosis in two-level three-phase PWM boost rectifier," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 3411-3423, Apr. 2018.

[19] L. F. Costa and M. Liserre, "Failure analysis of the dc-dc converter: a comprehensive survey of faults and solutions for improving reliability," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 42-51, Dec. 2018.

[20] J. Chen, C. Zhang, A. Chen, and X. Xing, "Fault-tolerant control strategies for T-type three-level inverters considering neutral-point voltage oscillations," *IEEE Trans. Ind. Electron*., vol. 66, no. 4, pp. 2837-2846, Apr. 2019.

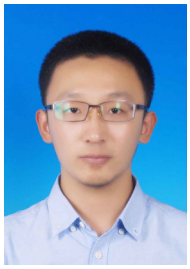
[21] E. Ribeiro, A. J. M. Cardoso, and C. Boccaletti, "Fault-tolerant strategy for a photovoltaic DC-DC converter," *IEEE Trans. Power Electron*., vol. 28, no. 6, pp. 3008-3018, Jun. 2013.

[22] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron*., vol. 29, no. 12, pp. 6319-6331, Dec. 2014.

[23] Y. Pan, C. Zhang, L. Du, A. Chen, and J. He, "Control method of hybrid fault tolerant for series resonant dual-active-bridge interfacing converters in DC distribution systems," *Automation of Electric Power Systems* (in Chinese), vol. 42, no. 20, pp. 130-137, Oct. 2018.

[24] R. W. A. A. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications, " *IEEE Trans. Ind. Appl*., vol. 27, no. 1, pp. 63-73, Jan./Feb. 1991.

[25] M. Zhang, X. Li, J. Liu, and H. Su, "Dual-mode LQR-feedforward optimal control for non-minimum phase boost converter," *IET Power Electron*., vol. 10, no. 1, pp. 92-102, 2017.



Yiwei Pan (S'19) received the B.S. degree in automation and M.S. degree in power electronics from Shandong University, Ji'nan, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree at Aalborg University, Aalborg, Denmark.

His current research interests include multilevel converters and distributed power generation.

Yongheng Yang (SM'17) received the B.Eng. degree in electrical engineering and automation from Northwestern Polytechnical University, Shaanxi, China, in 2009 and the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 2014.

He was a postgraduate student at Southeast University, China, from 2009 to 2011. In 2013, he spent three months as a Visiting Scholar at Texas A&M University, USA. Currently, he is an Associate Professor with the Department of Energy Technology, Aalborg University, and the Vice Program Leader for the research program on photovoltaic systems. His current research is on the integration of grid-friendly photovoltaic systems with an emphasis on the power electronics converter design, control, and reliability.

Dr. Yang is the Chair of the IEEE Denmark Section. He serves as an Associate Editor for several prestigious journals, including the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, and the IEEE Industry Applications Society Publications. He is a Subject Editor of the *IET Renewable Power Generation* for Solar Photovoltaic Systems, including MPPT. Dr. Yang was the recipient of the 2018 *IET Renewable Power Generation* Premium Award and was an Outstanding Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2018.

Jinwei He (M'14) received the B.S. degree from Southeast University, Nanjing, China, the M.S. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, and the Ph.D. from the University of Alberta, Canada, all in Electrical Engineering, in 2005, 2008, and 2013, respectively. In September 2015, he joined Tianjin University, China, where he currently is a Professor. His research interests are power electronics for microgrid and distributed power generation.

Dr. He serves as an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS and *IET Energy Systems Integration*. Dr. He received the second prize paper award of IEEE TRANSACTIONS ON POWER ELECTRONICS in 2014.

Ariya Sangwongwanich (S'15–M'19) received the M.Sc. and Ph.D. degree in energy engineering from Aalborg University, Denmark, in 2015 and 2018, respectively. Currently, he is working as a Postdoc Fellow at the Department of Energy Technology, Aalborg University.

He was a Visiting Researcher with RWTH Aachen, Aachen, Germany from September to December 2017. His research interests include control of grid-connected converter, photovoltaic systems, reliability in power electronics and multilevel converters. He has co-authored the book – Advanced in Grid-Connected Photovoltaic Power Conversion Systems. In 2019, he received the Danish Academy of Natural Sciences' Ph.D. prize and the Spar Nord Foundation Research Award for his Ph.D. thesis. Dr. Sangwongwanich also serves as the Chair of the IEEE Student Branch at Aalborg University.

Chenghui Zhang (M'14–SM'18) received his Bachelor and Master Degrees in automation engineering from Shandong University of Technology, Jinan, China, in 1985 and 1988, and the Ph.D. degree in control theory and operational research from Shandong University, Jinan, in 2001, respectively. In 1988, he joined Shandong University, where he is currently a Professor of School of Control Science and Engineering at Shandong University, the chief manager of Power Electronic Energy-saving Technology & Equipment Research Center of Education Ministry, a Specially Invited Cheung Kong Scholars Professor by China Ministry of Education, and a Taishan Scholar Special Adjunct Professor. He is also one of State-level candidates of "the New Century National Hundred, Thousand and Ten Thousand Talent Project", the academic leader of Innovation Team of Ministry of Education, and the chief expert of the National "863" high technological planning.

His research interests include optimal control of engineering, power electronics and motor drives, energy-saving techniques, and time-delay systems.

Yang Liu (M'12–SM'17) was born in Hubei Province, China, in 1979. He received the M.E. and Ph.D. degrees in control science and engineering from the Department of Control Science and Engineering, School of Automation, Huazhong University of Science and Technology (HUST), Wuhan, China, in 2005 and 2009, respectively. He is currently an associate professor in the School of Artificial Intelligence and Automation, HUST. His research interests include power electronics using SiC and GaN, high performance ac motor drives, and active harmony filter topology and control.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 32 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he serves a President of IEEE Power Electronics Society. He is Vice-President of the Danish Academy of Technical Sciences too.

He is nominated in 2014-2019 by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.